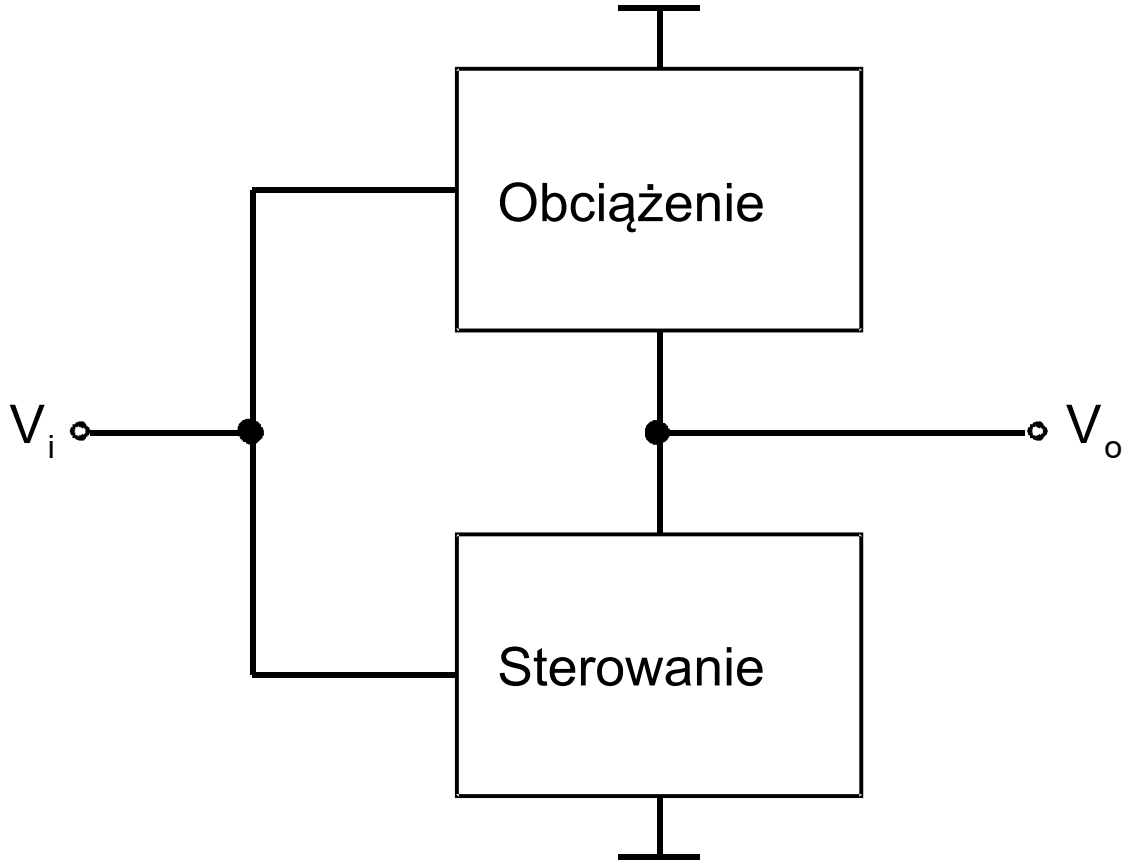
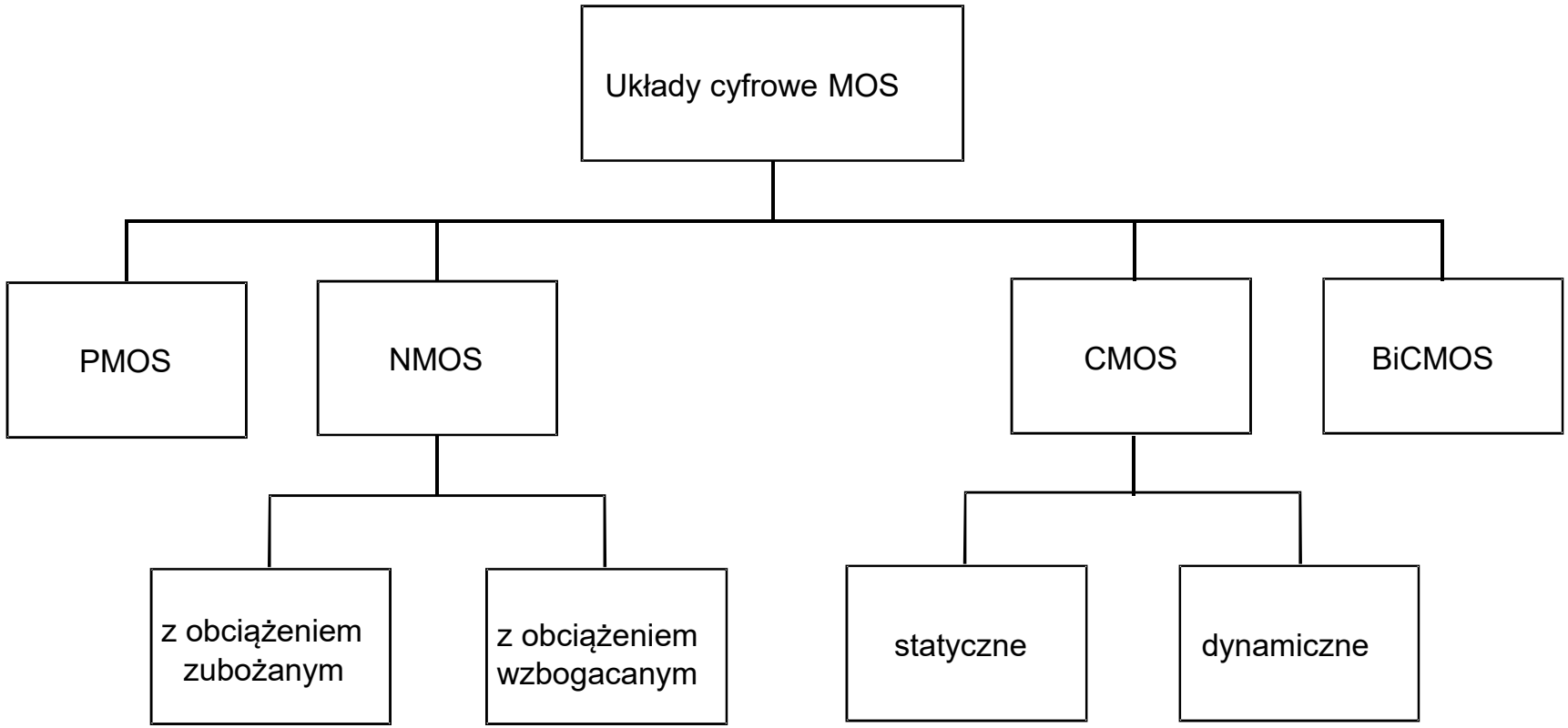
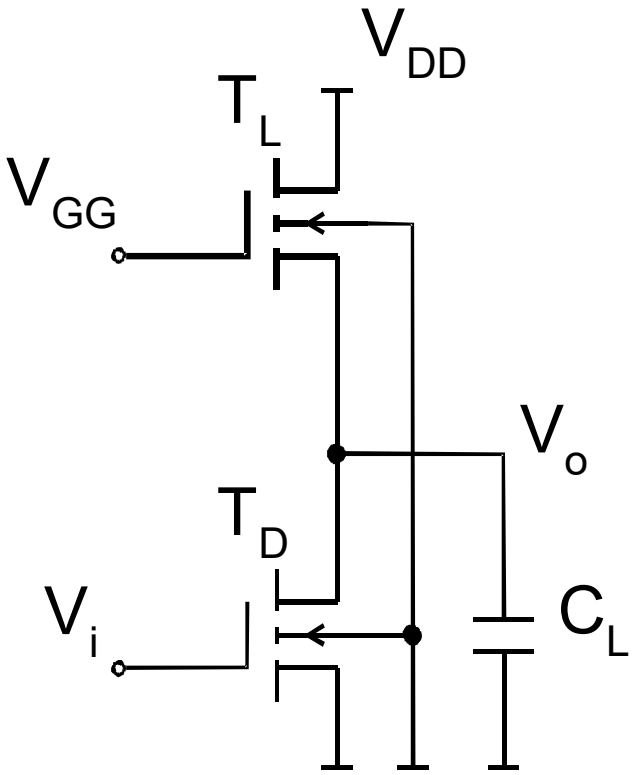
Ogólny schemat inwertera MOS



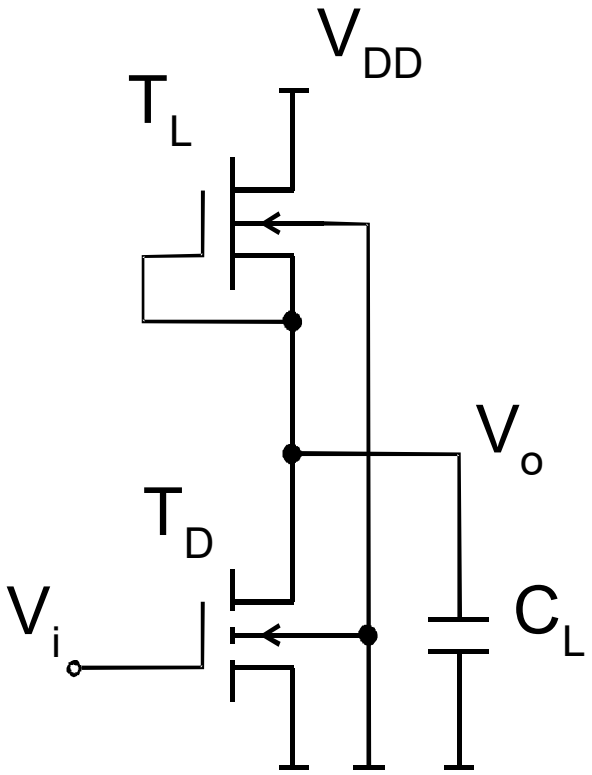
Rodzaje cyfrowych układów scalonych MOS



Bramki NMOS

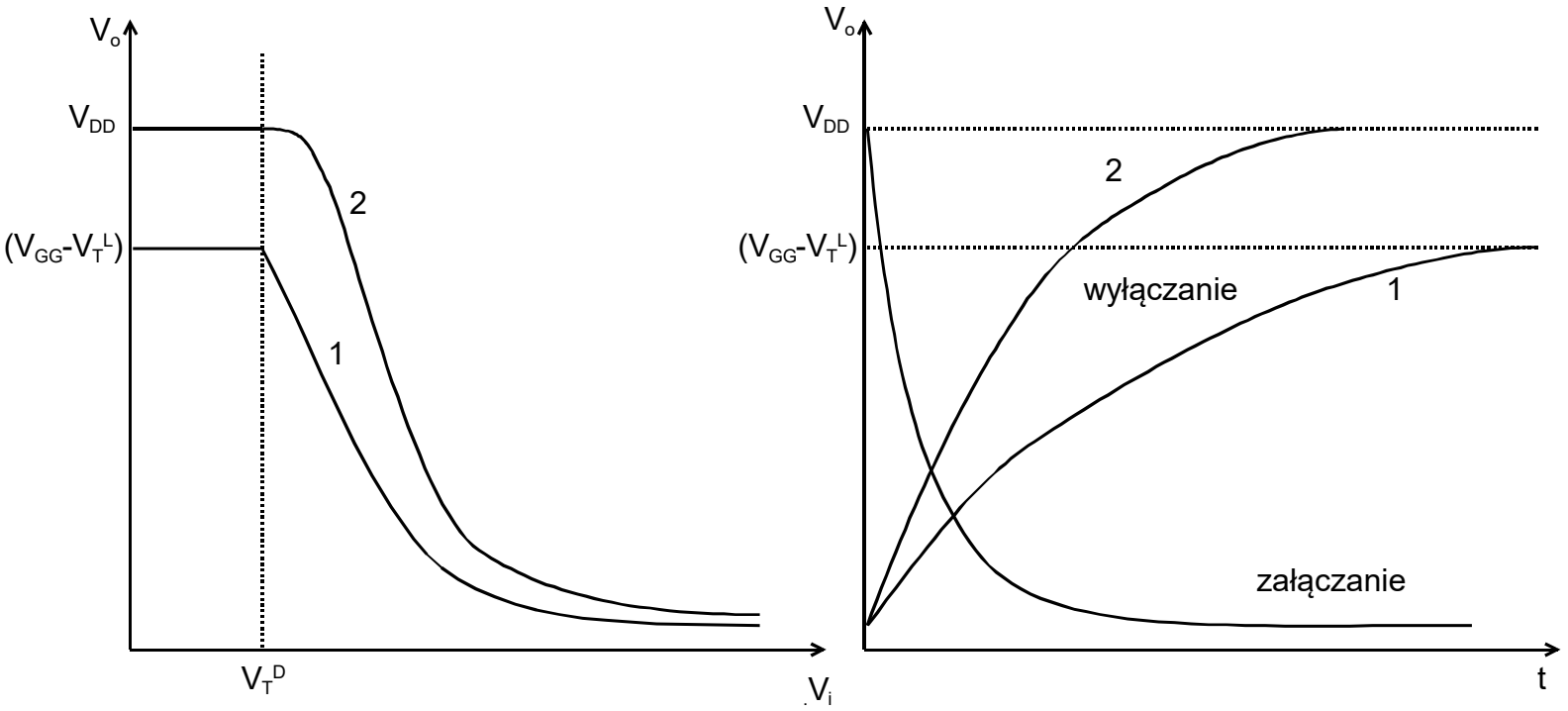


z obciążeniem typu wzbogacanego



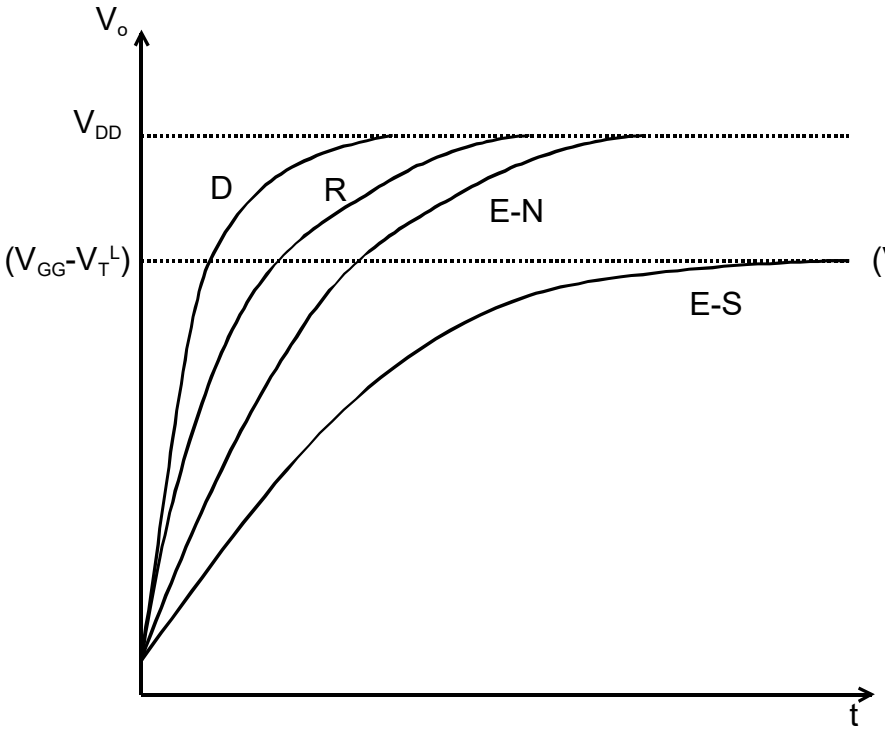
z obciążeniem typu zubożanego

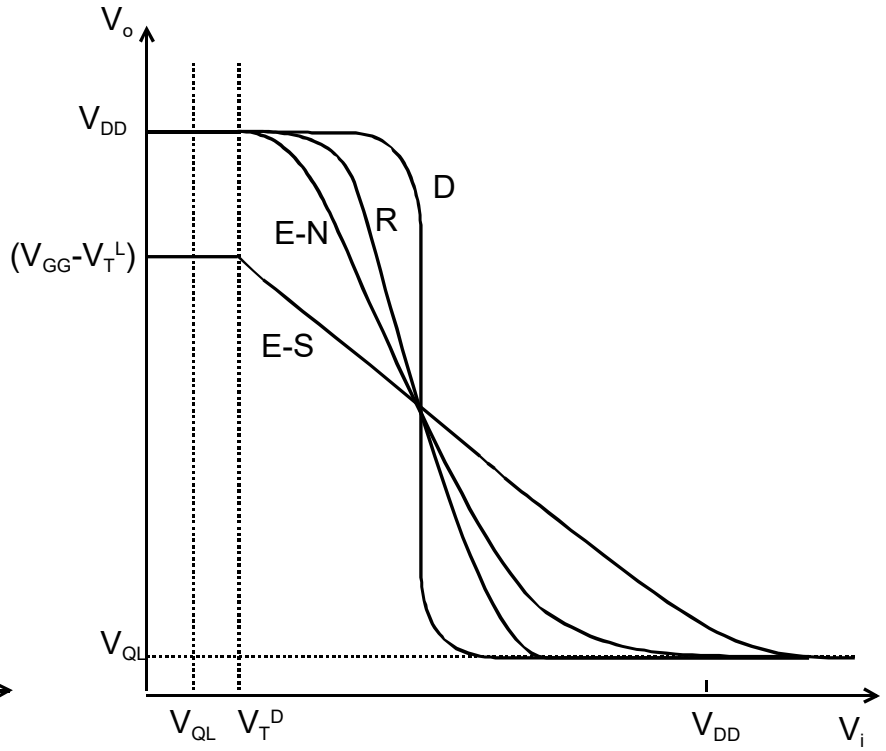
Bramki NMOS z obciążeniem typu wzbogacanego



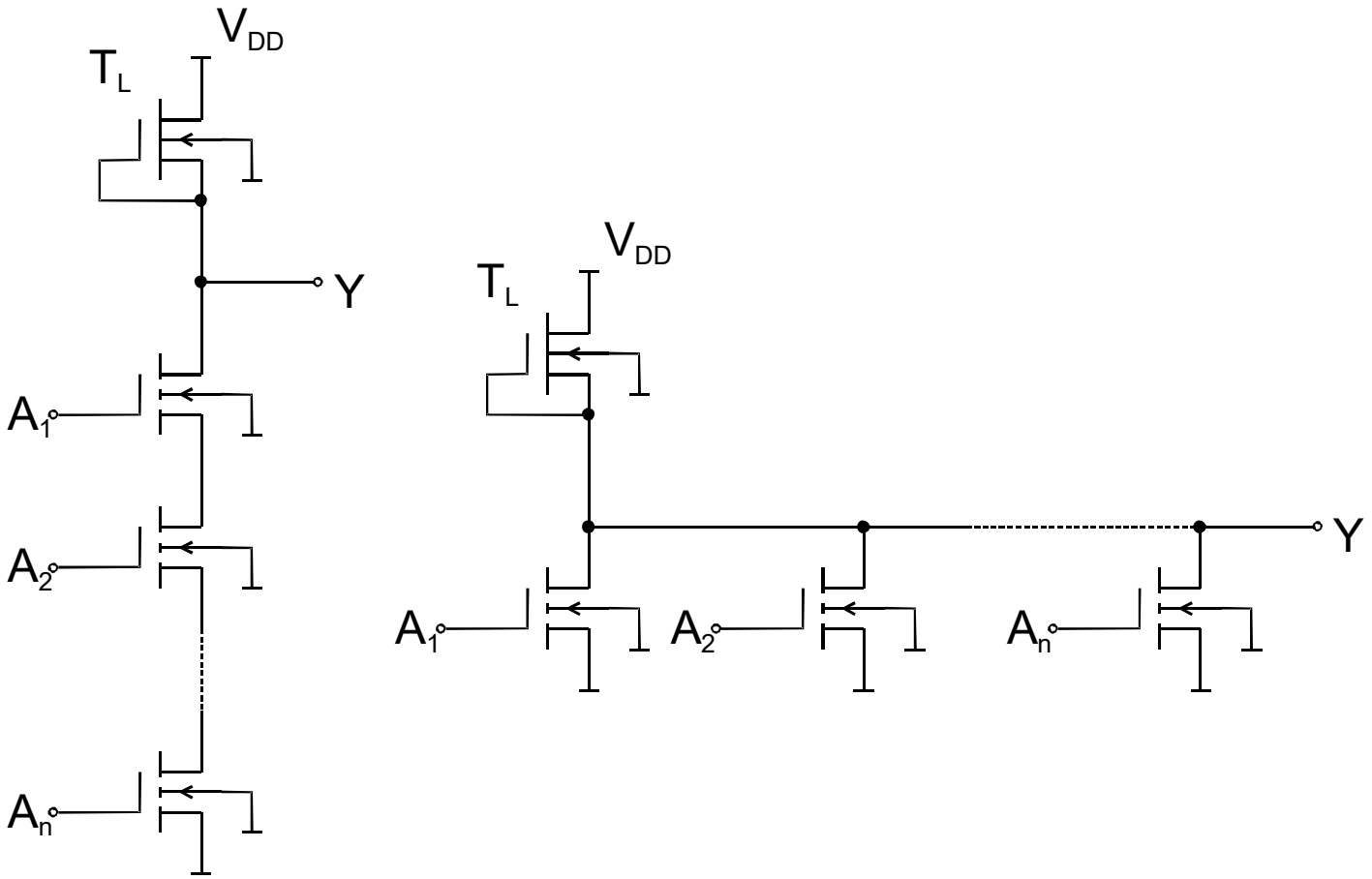
1. VGG<VDD+VTL - tranzystor obciążający pracuje w zakresie nasycenia
2. VGG≥VDD+VTL - tranzystor obciążający pracuje w zakresie nienasycenia

Porównanie bramek NMOS z różnymi obciążeniami

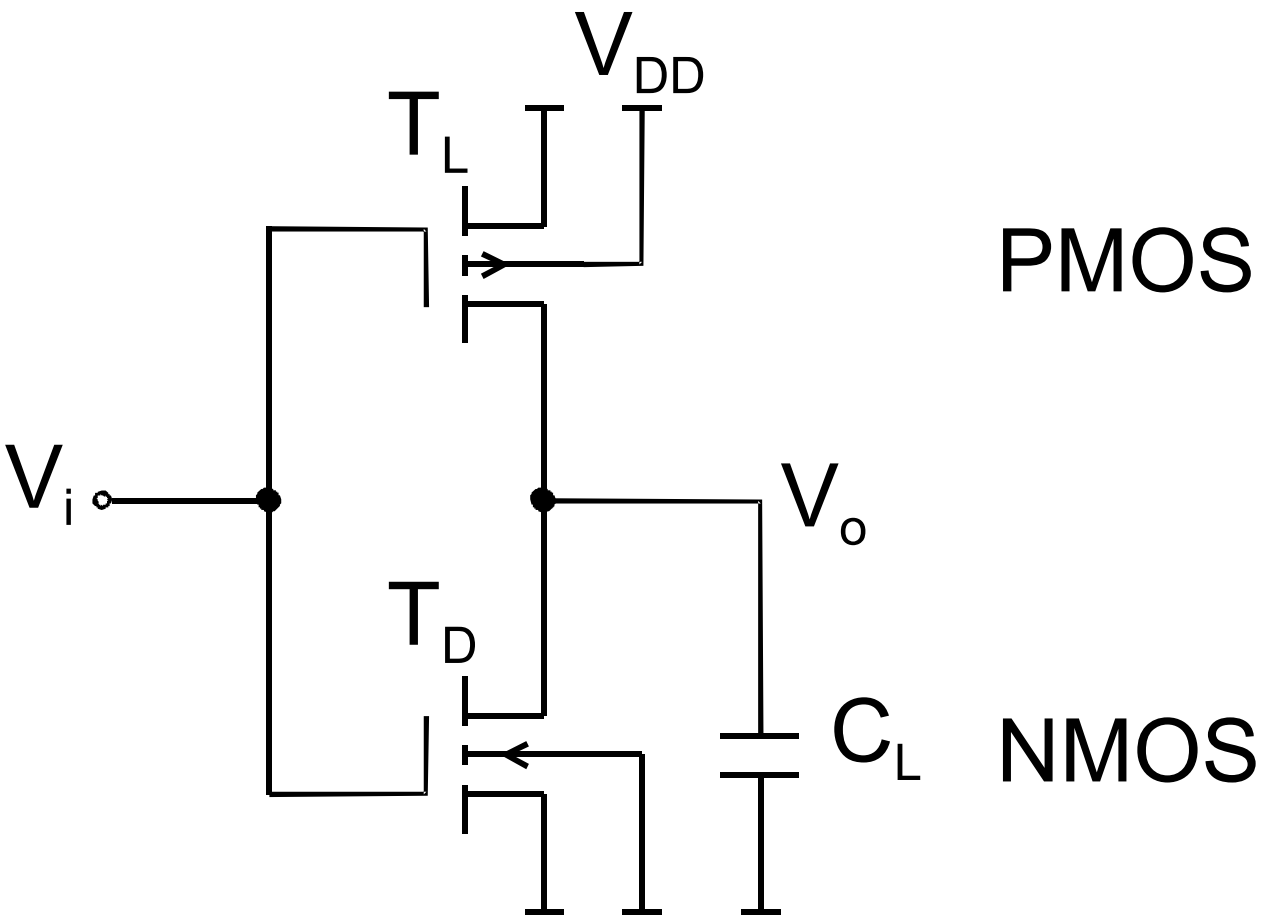




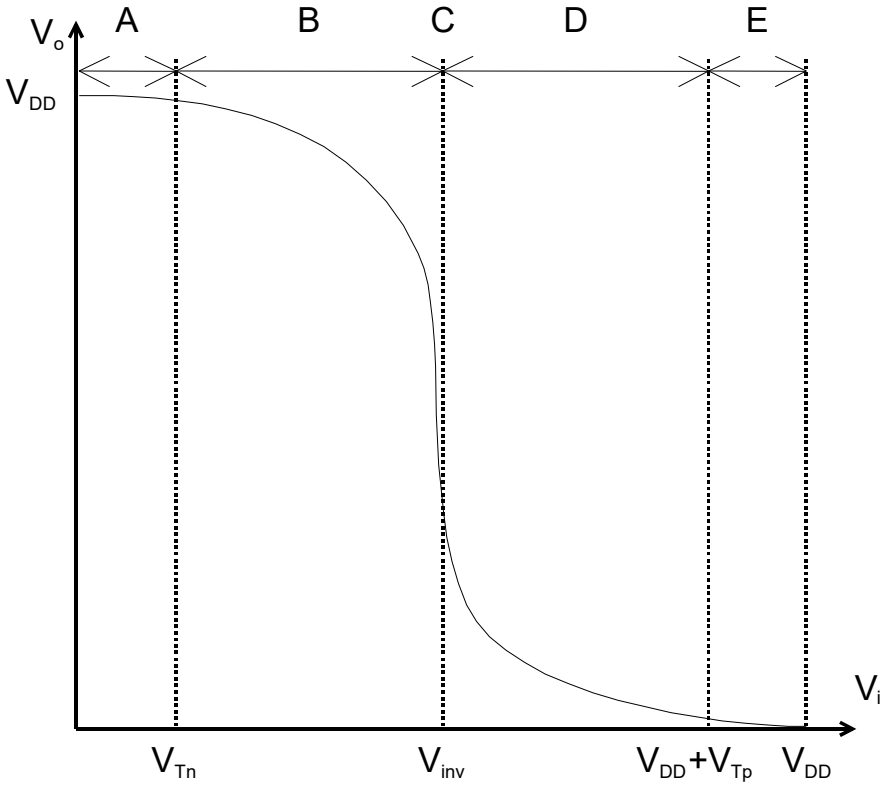
Bramki logiczne NMOS: NAND i NOR

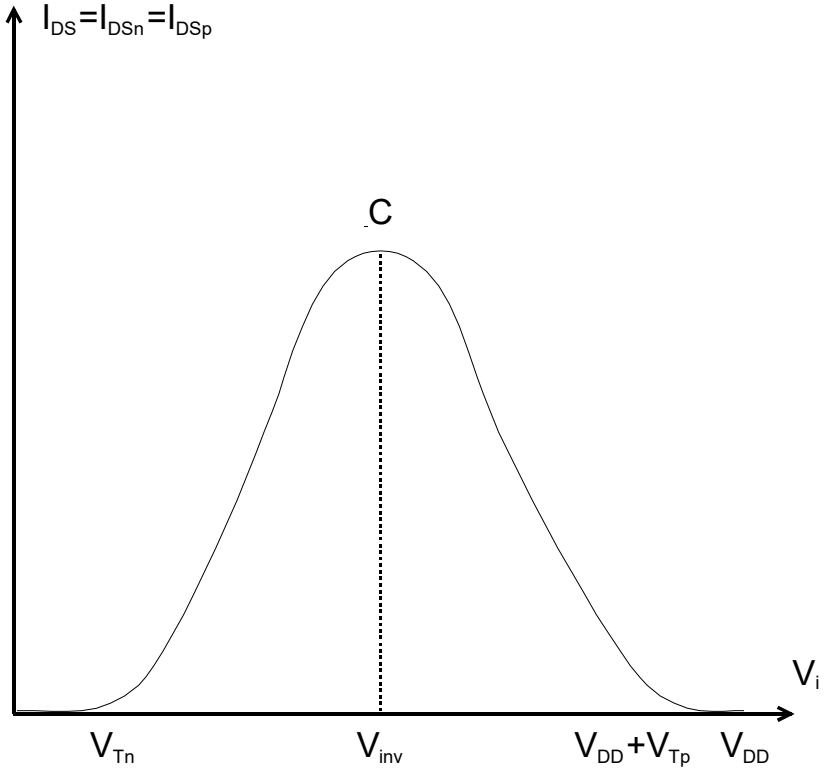


Inwerter CMOS

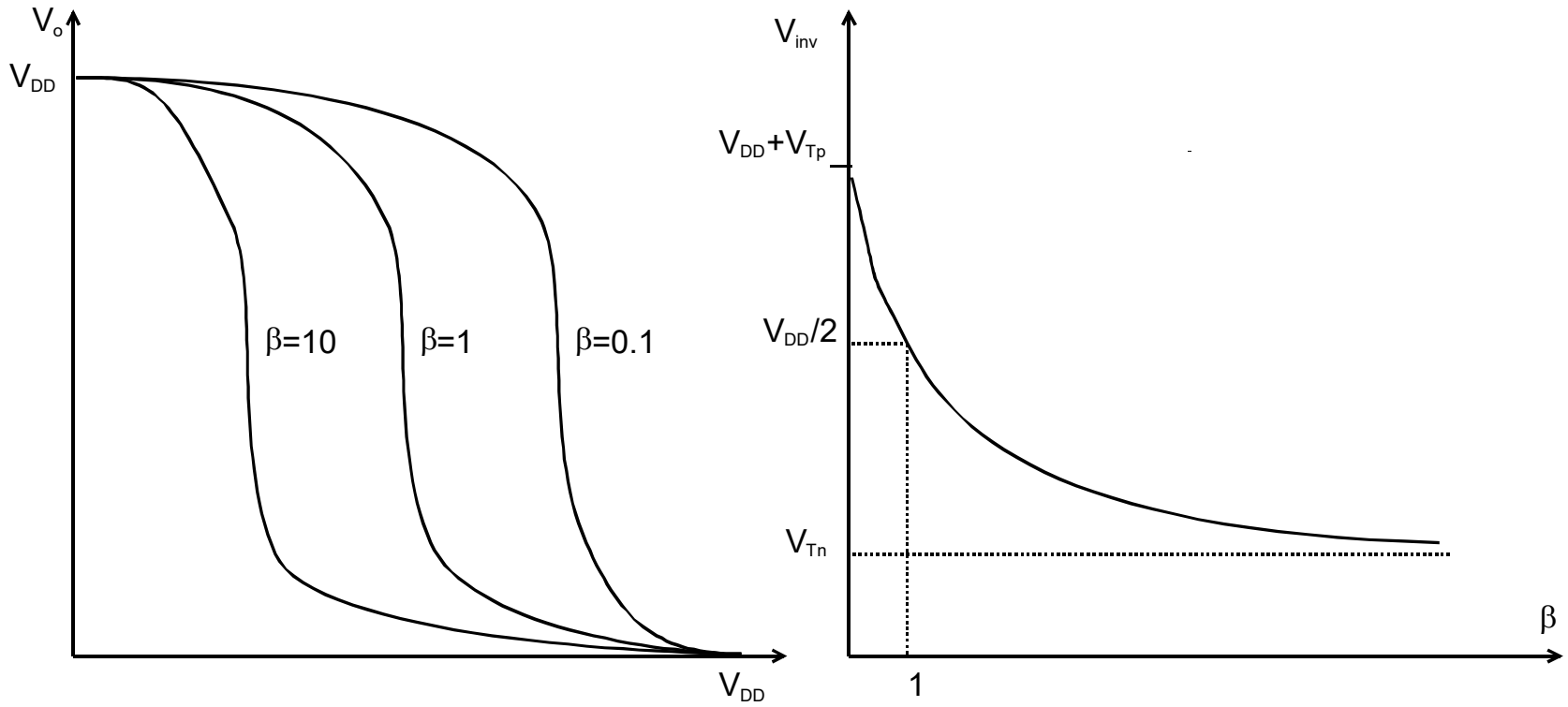


Charakterystyka przejściowa i prąd inwertera CMOS

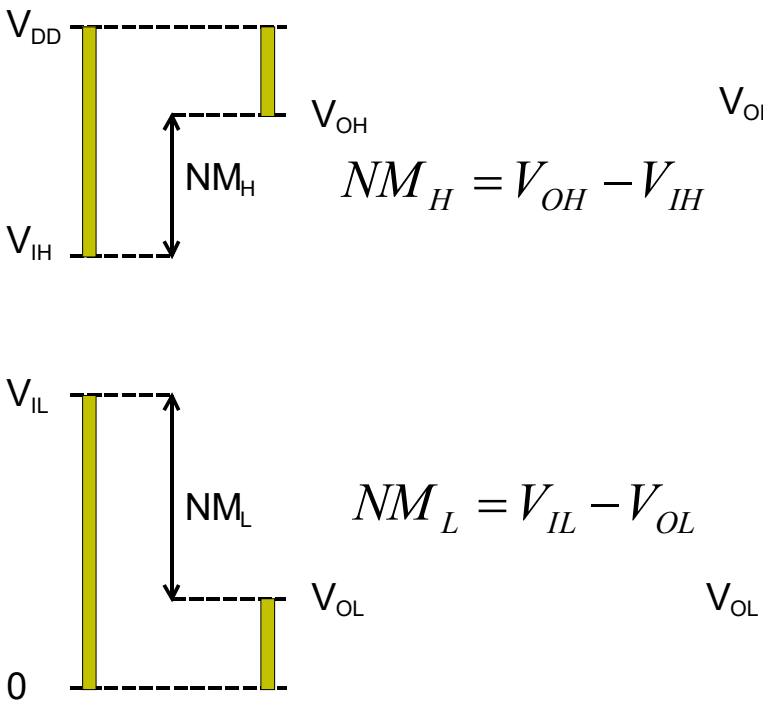




Wpływ współczynnika β na charakterystykę przejściową i napięcie progowe inwertera CMOS

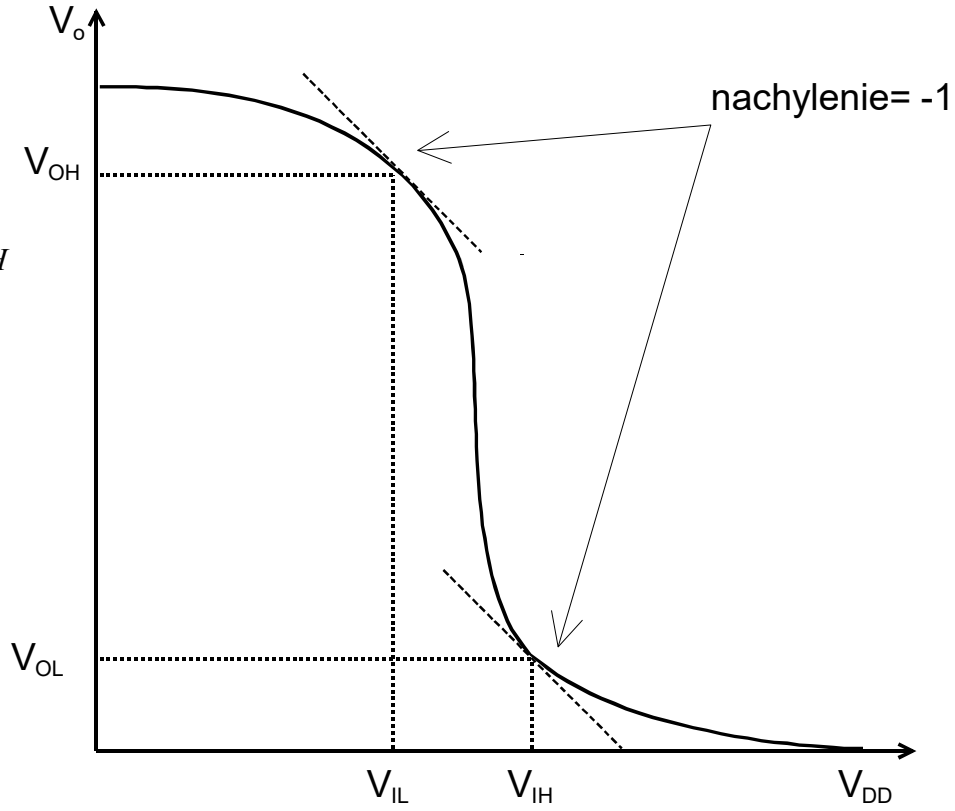


Definicja marginesów szumów

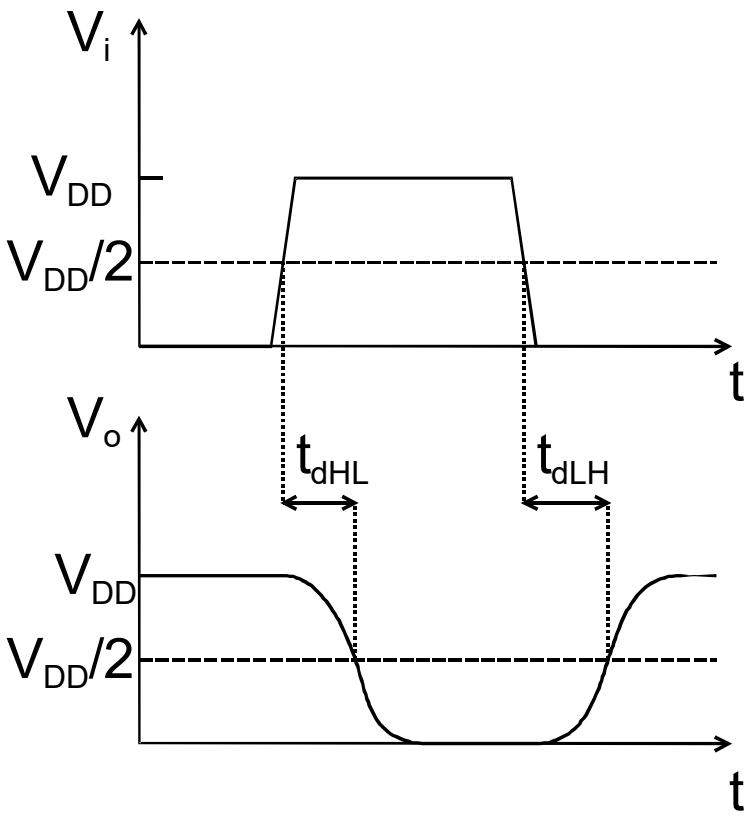


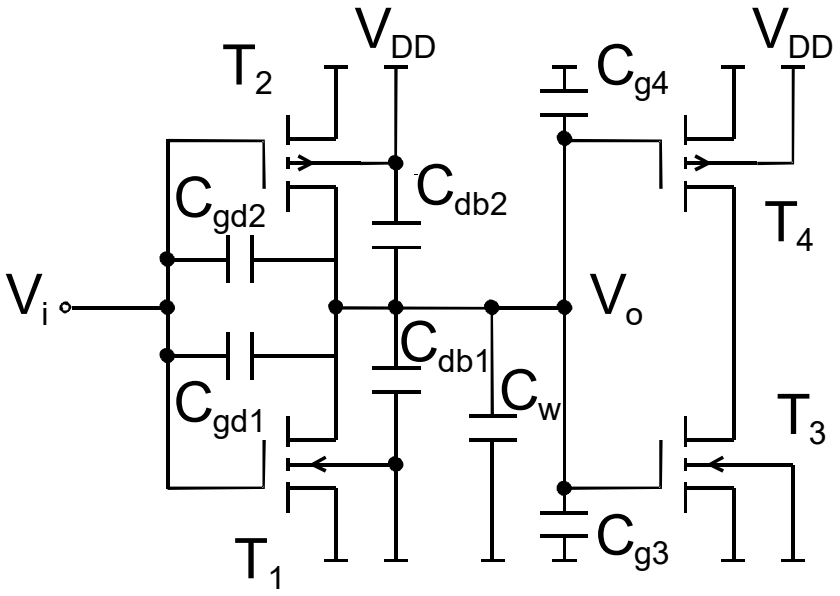
$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$

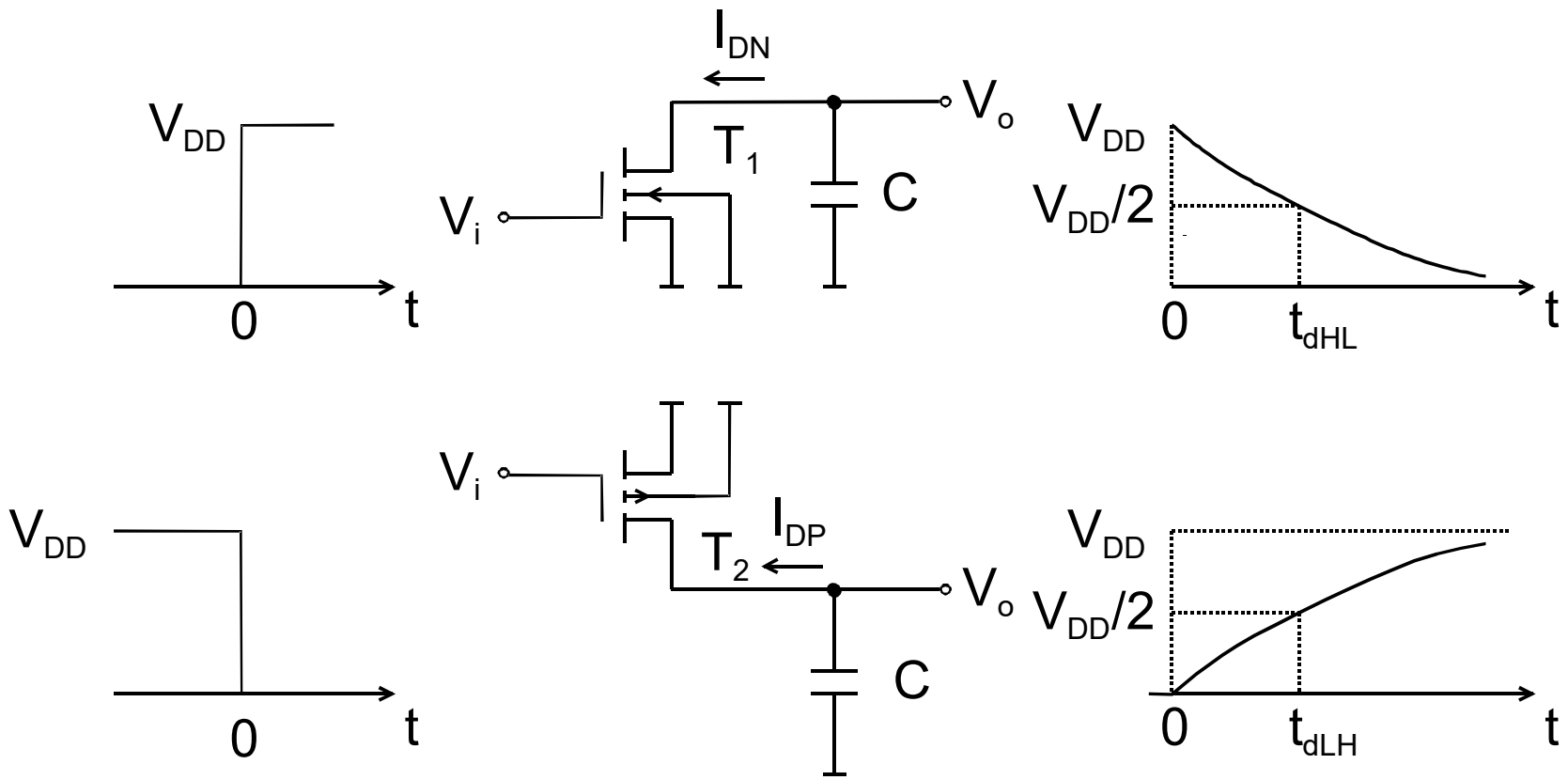


Opóźnienia wnoszone przez inwerter CMOS

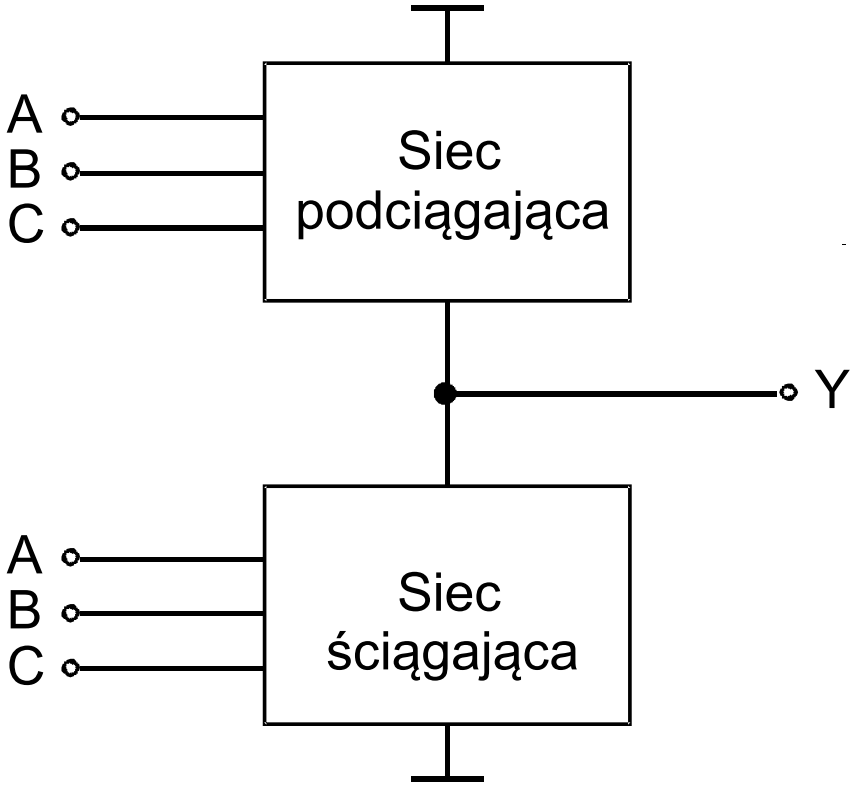




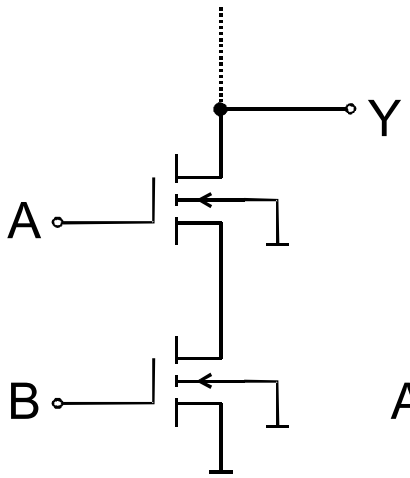
Obliczanie czasów opóźnień t_{dHL} i t_{dLH}



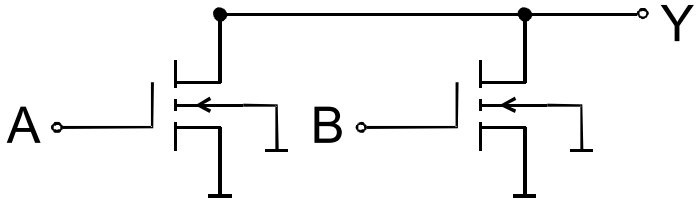
Ogólny schemat bramki CMOS



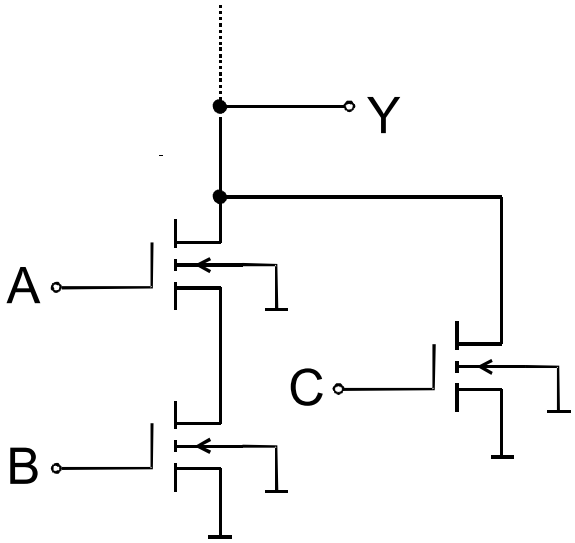
Schematy sieci ściągających w bramkach CMOS



$Y=\overline{AB}$

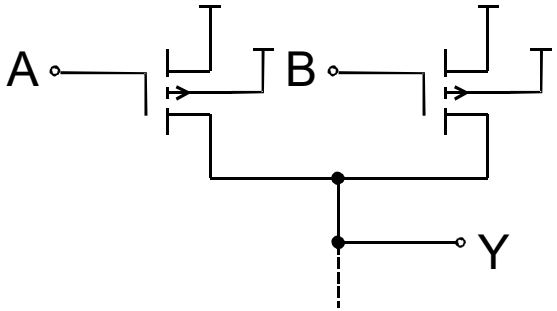


$Y=\overline{A+B}$

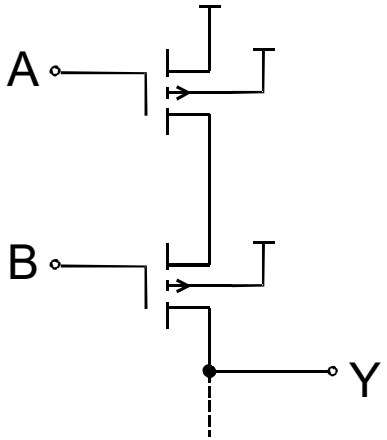


$Y=\overline{AB+C}$

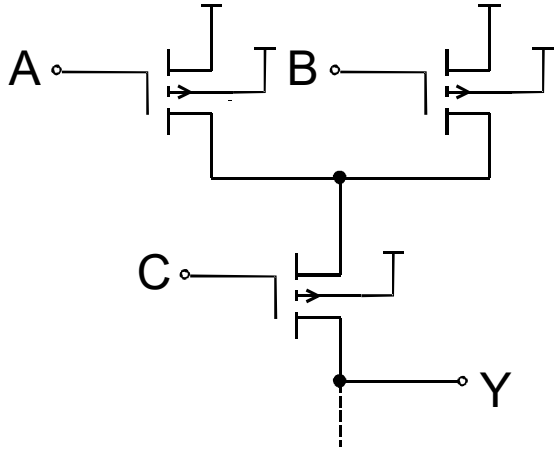
Schematy sieci podciągających w bramkach CMOS



$Y=\overline{AB}$

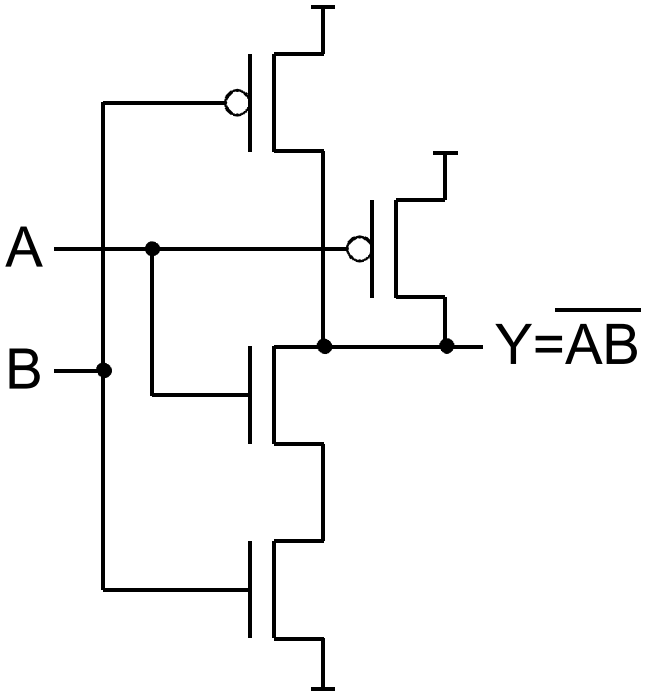


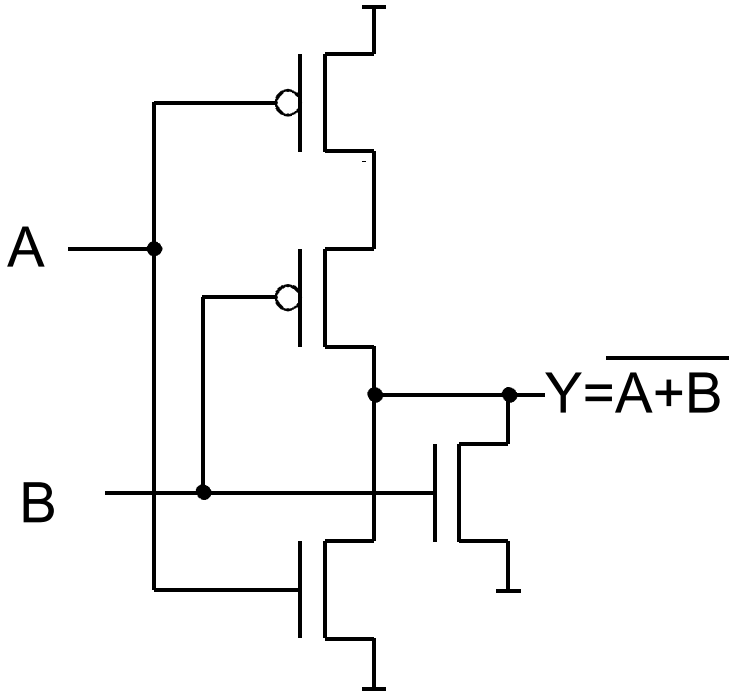
$Y=\overline{A+B}$



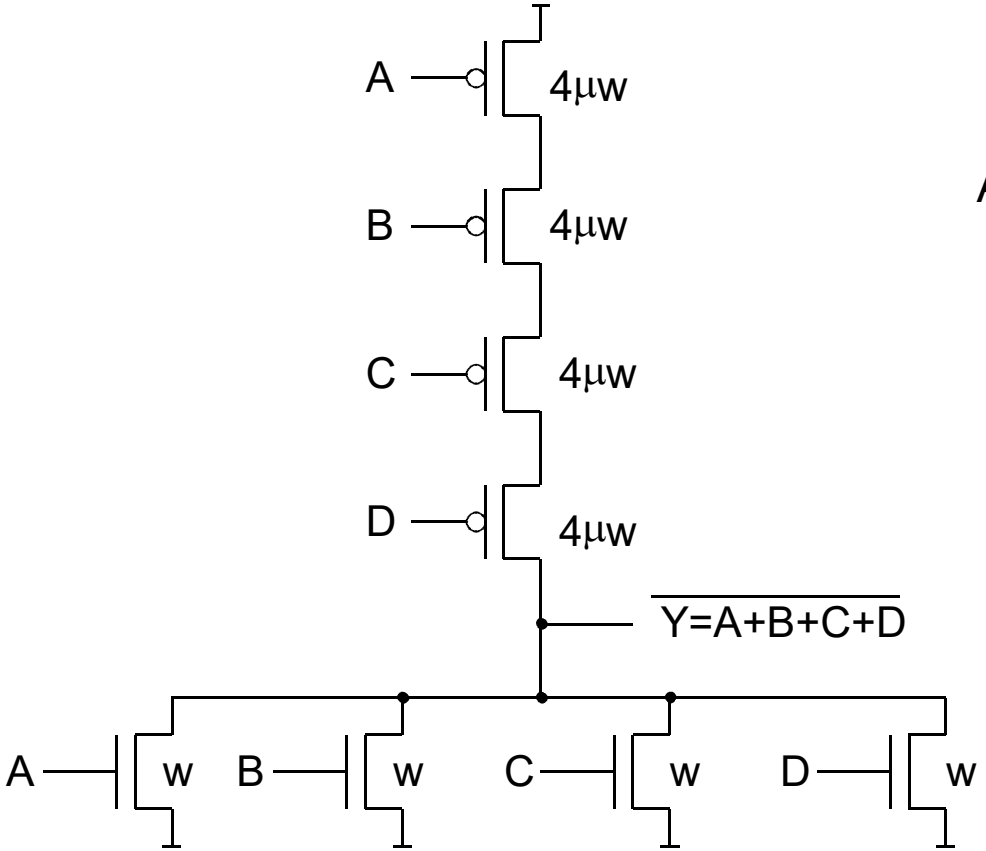
$Y=\overline{AB+C}$

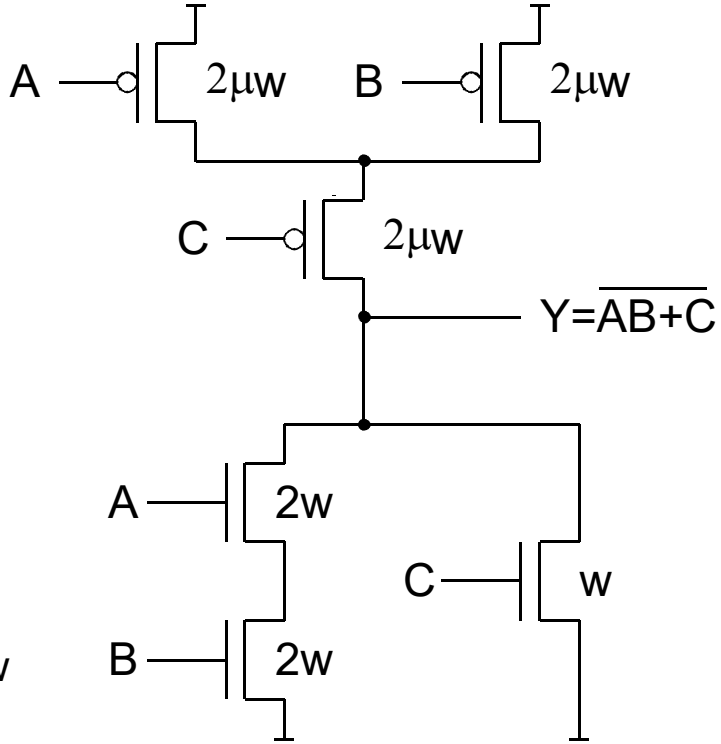
Bramki CMOS: NAND i NOR



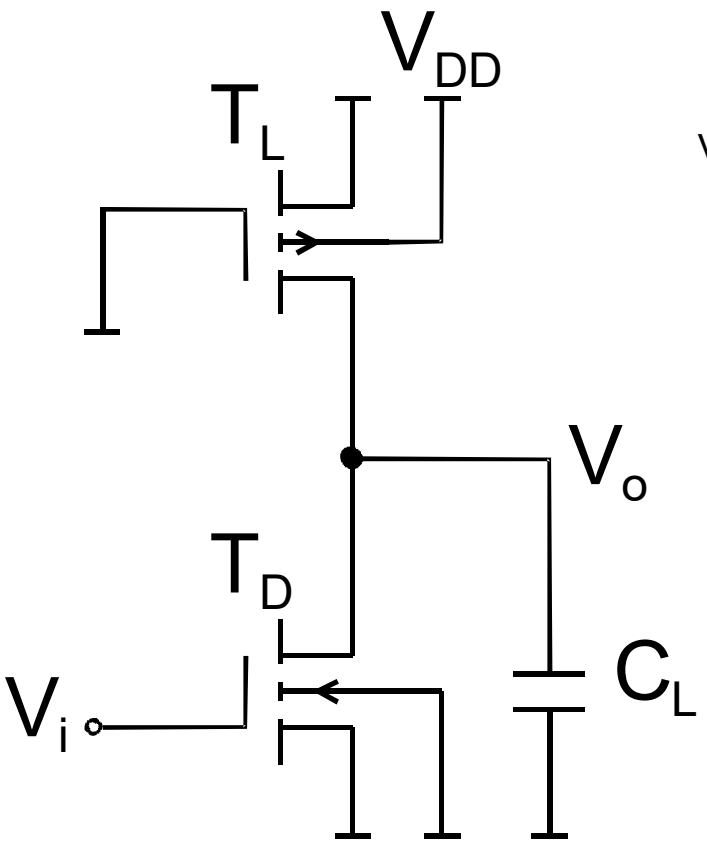


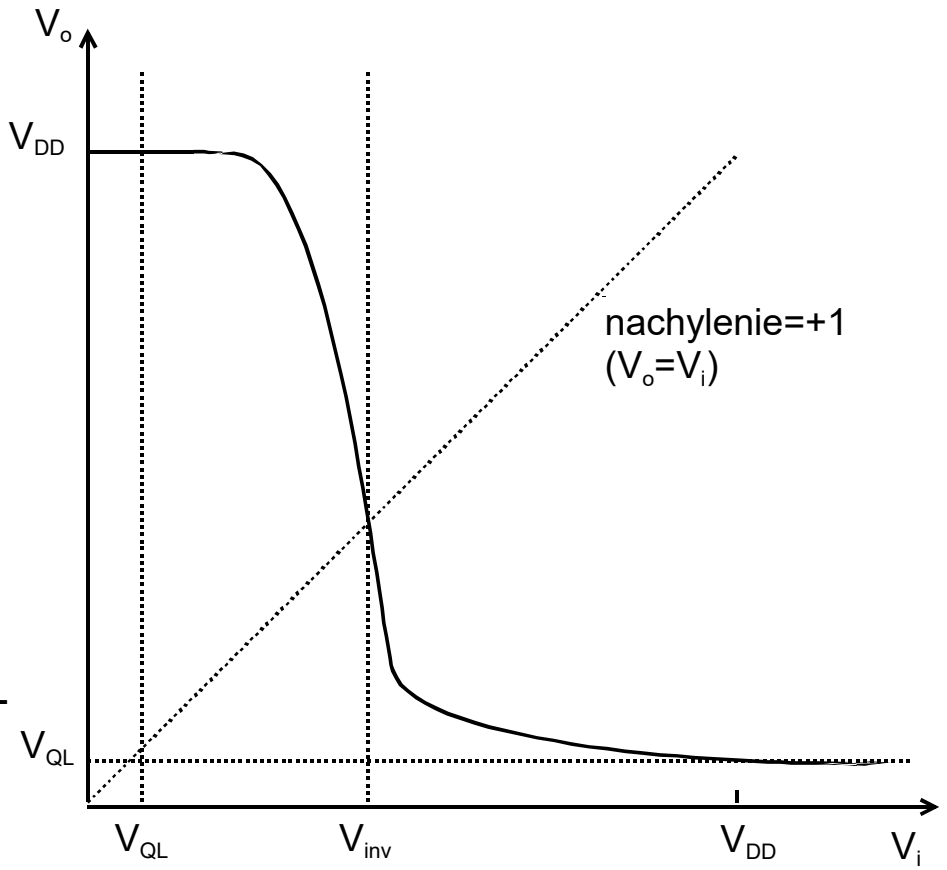
Dobór szerokości tranzystorów w bramkach CMOS



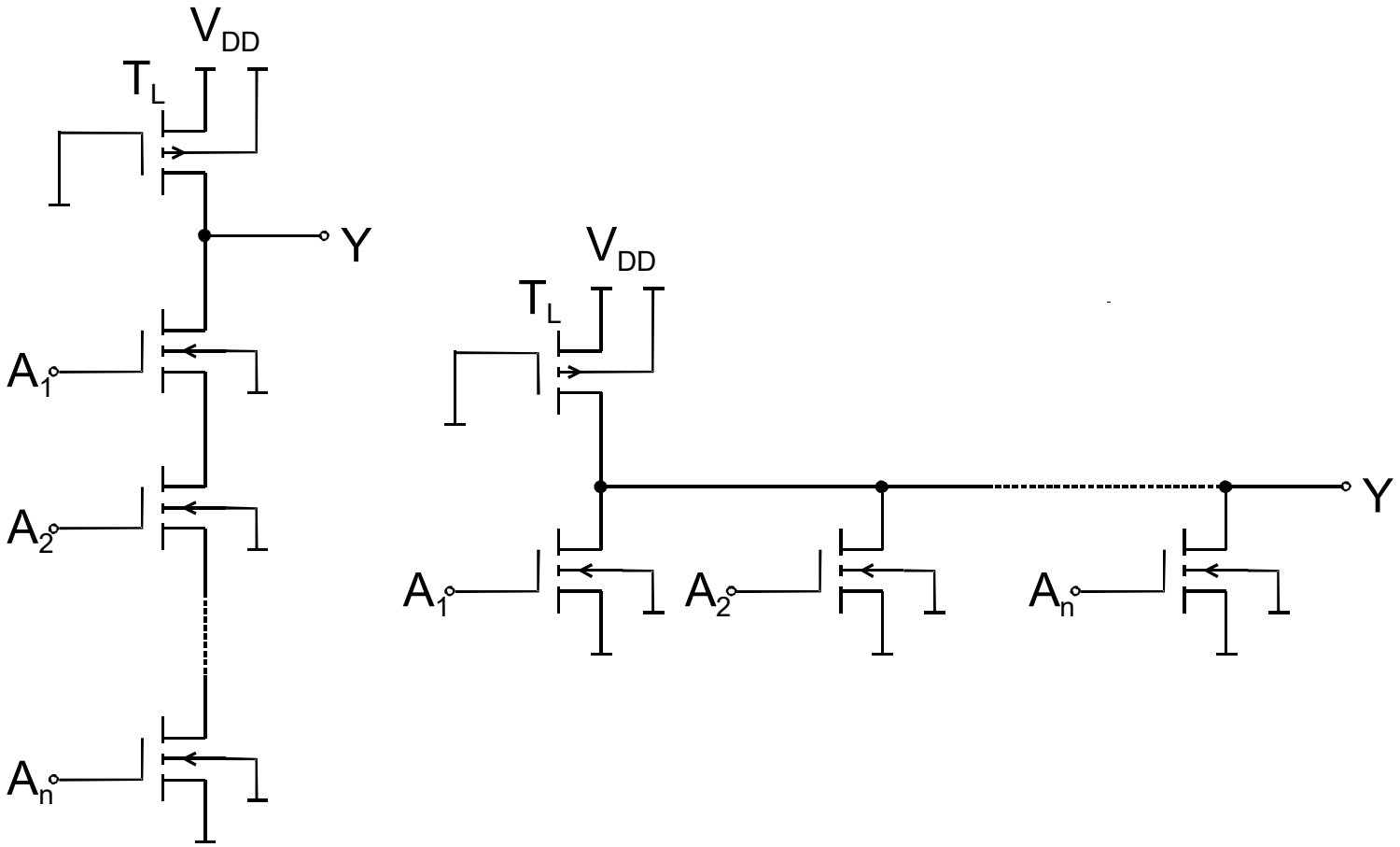


Inwerter pseudo-NMOS

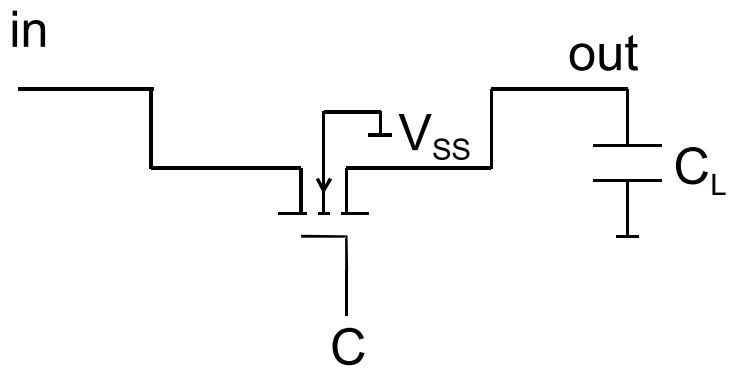


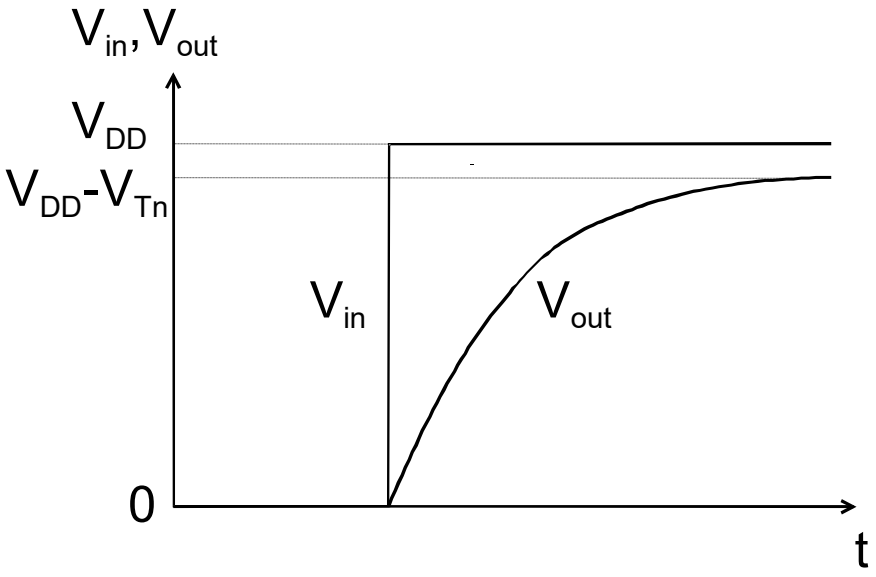


Bramki pseudo-NMOS: NAND i NOR

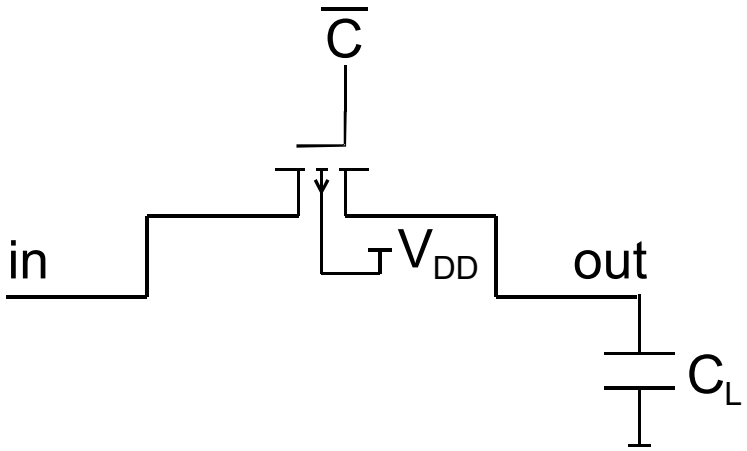


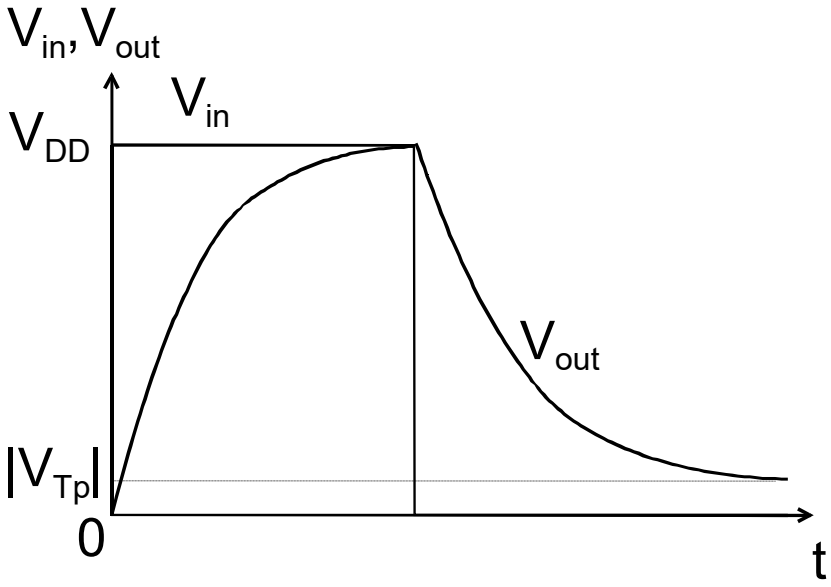
Tranzystor NMOS jako klucz



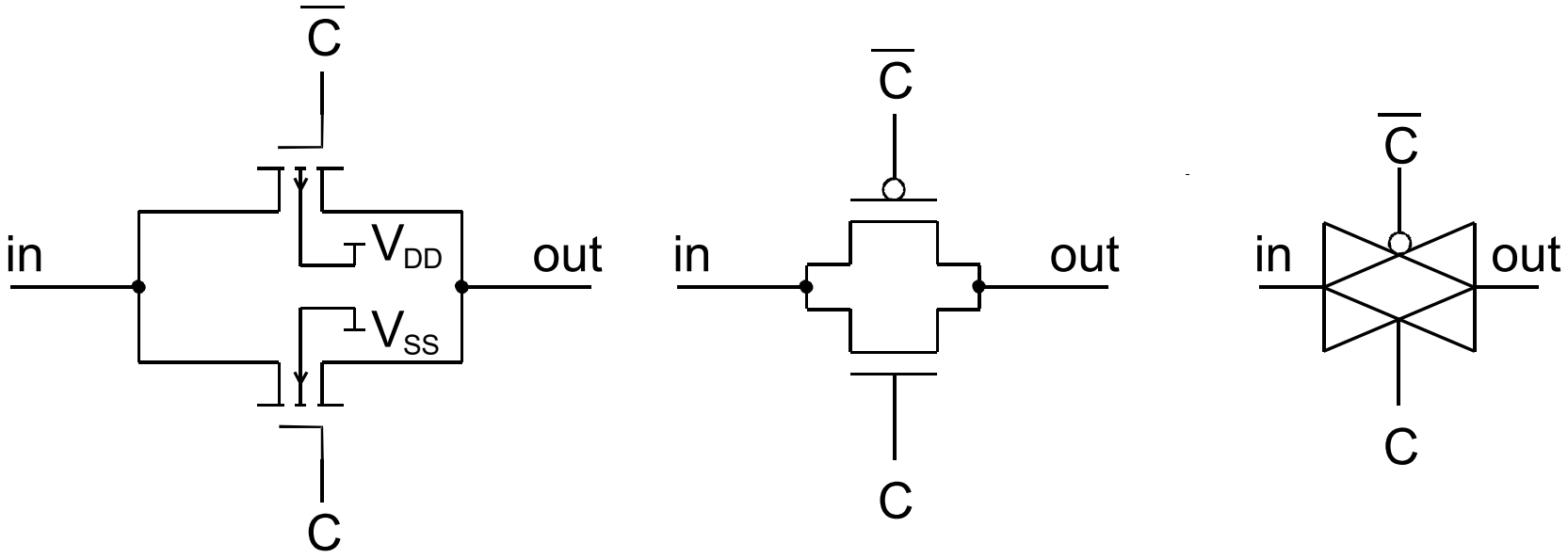


Tranzystor PMOS jako klucz

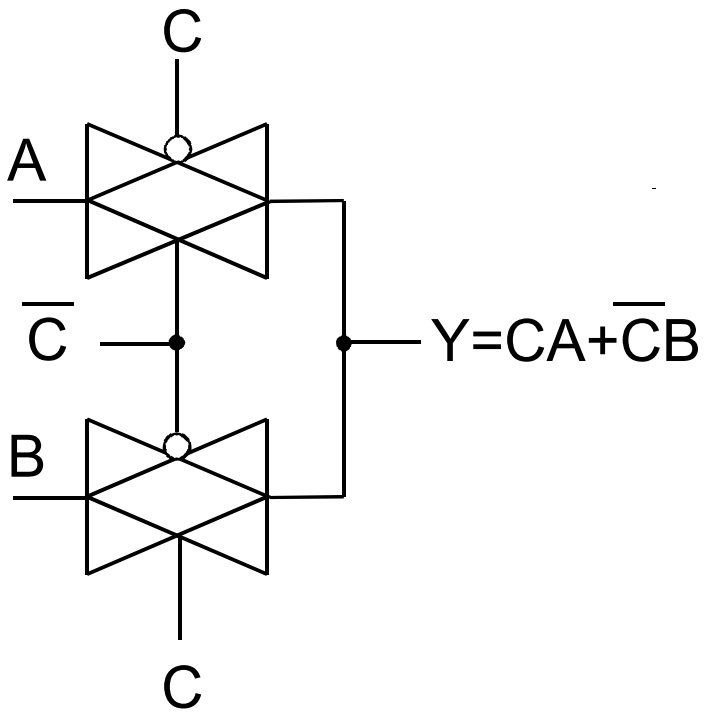




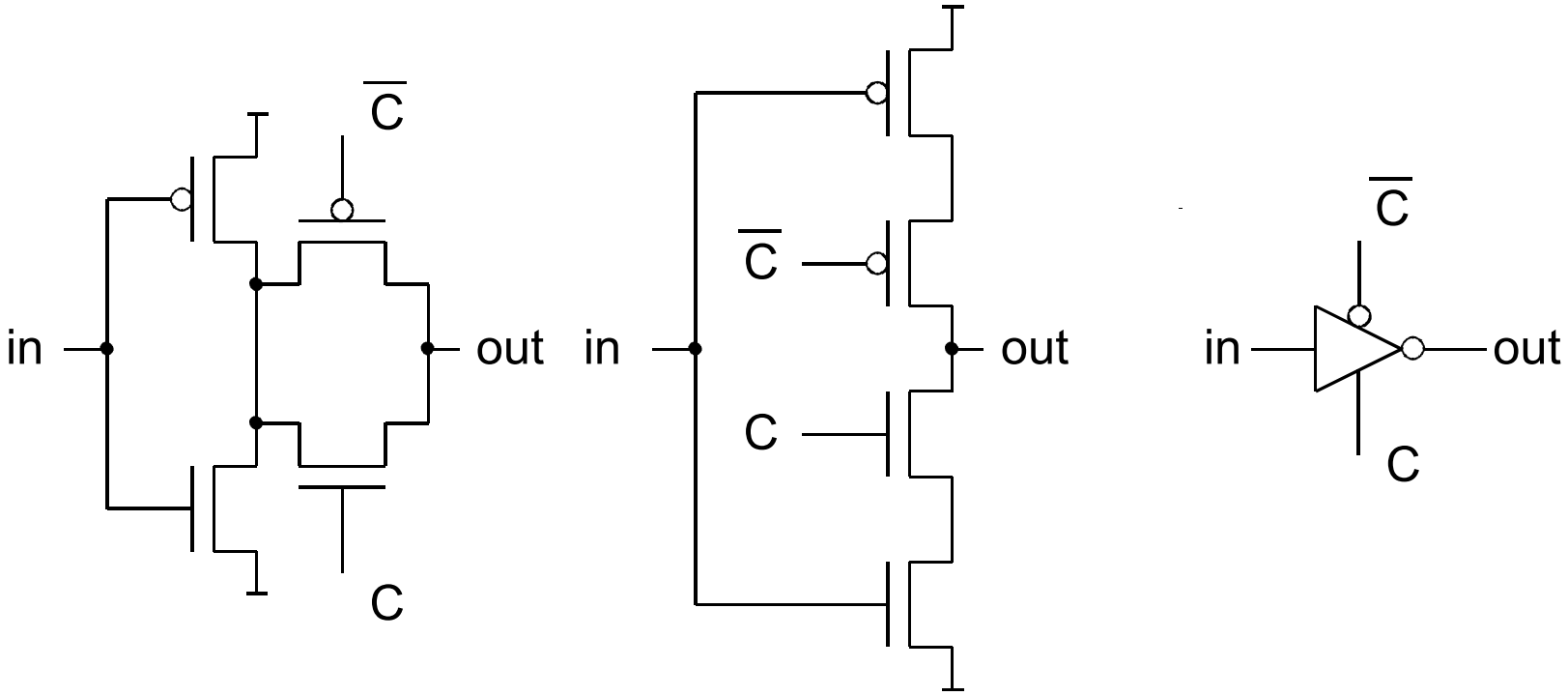
Bramka transmisyjna CMOS



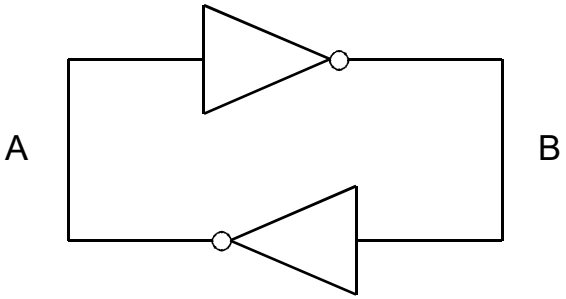
Dwuwejściowy multiplekser z bramek transmisyjnych

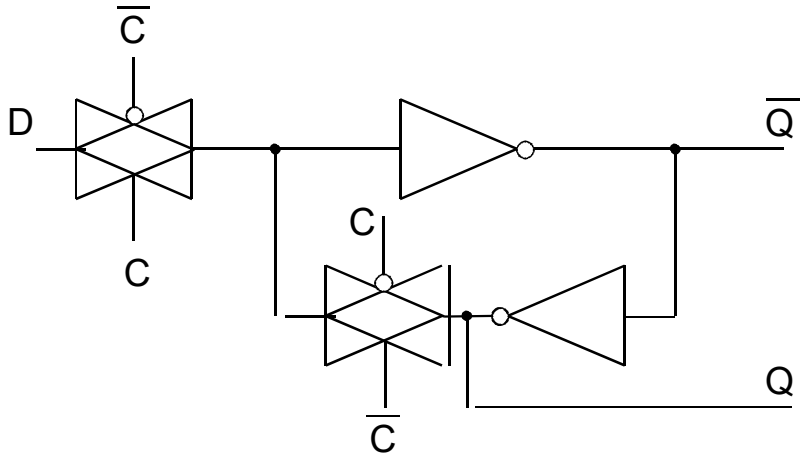


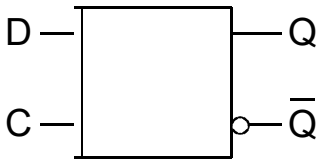
Inwerter trójstanowy

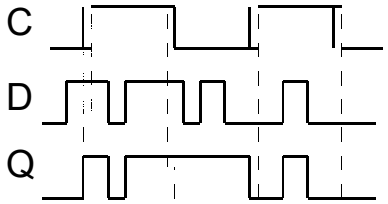


Przerzutnik D wyzwalany poziomem

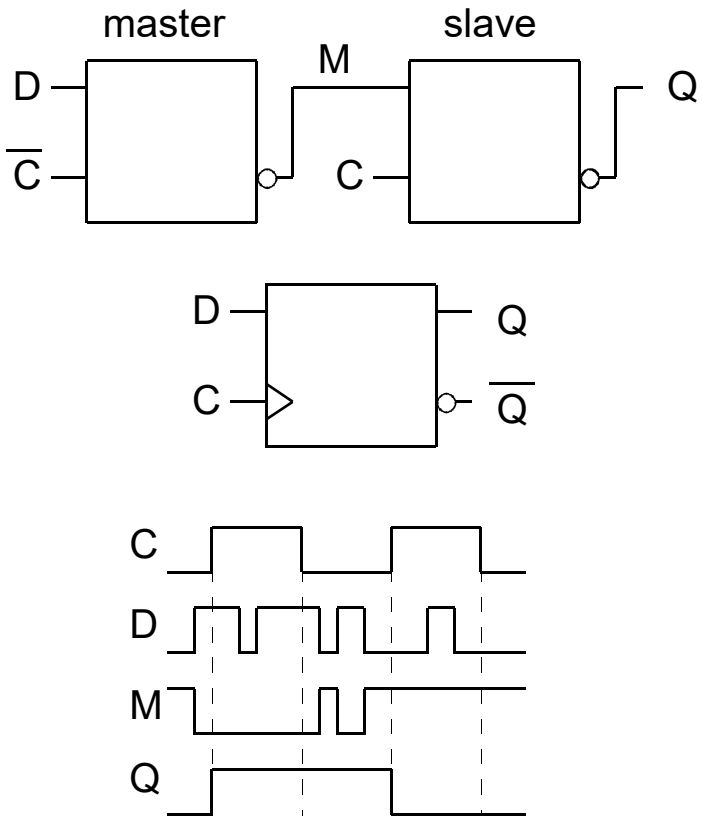




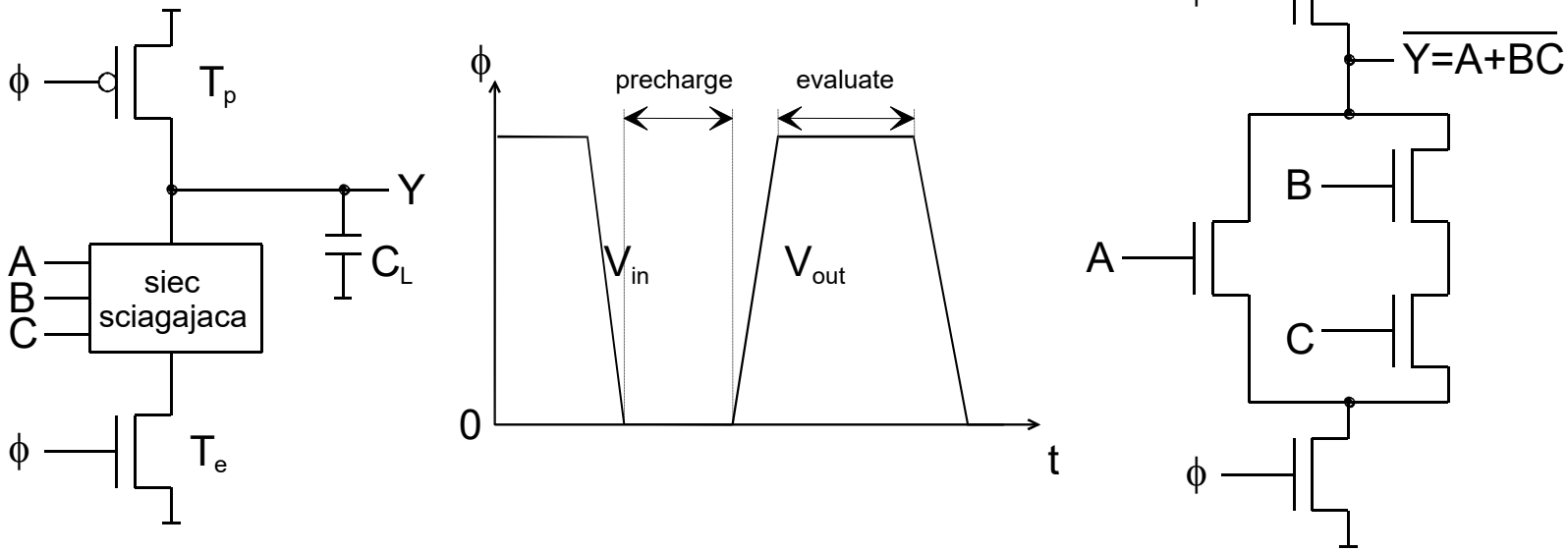




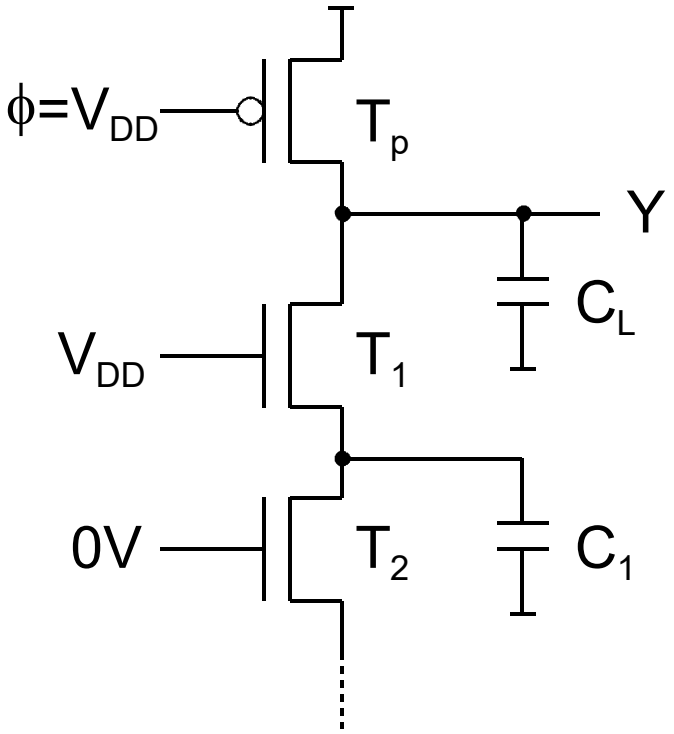
Przerzutnik D wyzwalany zboczem



Bramki dynamiczne



„Charge sharing” czyli zjawisko podziału ładunku



Łączenie bramek dynamicznych