CT8020
TrueSpeech®
## *G.723.1 Co-Processor*

Introduction

The CT8020 is a TrueSpeech co-processor which performs full duplex speech compression and de-compression functions. It provides speech compression for H.323 and H.324 Multimedia Visual Telephony / Video Conferencing products, and DSVD Modems (Digital Simultaneous Voice and Data) for use over standard PSTN phone line connections. TrueSpeech 8.5 is compatible with Microsoft Sound System 2.0, and is a standard part of Windows® 95. TrueSpeech 6.3 and 5.3 are fully compatible with the ITU-T G.723.1 speech compression standard specified under H.324 and H.323. The CT8020 supports TrueSpeech compressed data rates of 8.5, 6.3, 5.3, 4.8 and 4.1 Kbps. In DSVD Modems and Video Conferencing applications, the CT8020 device is designed to co-exist with the modem data pump ICs (and video compression device) to provide the speech compression/de-compression functions under the control of the host controller. In addition, the Acoustical Echo Canceller feature complements the TrueSpeech functions of this device by providing hands-free operation concurrently with TrueSpeech operation.

The TrueSpeech algorithm delivers highly compressed speech without compromising the speech quality. TrueSpeech 6.3 has a MOS score of 3.9 while running at 6.3 Kbps. TrueSpeech 6.3 with 6.3 and 5.3 kbps rates, has been approved as G.723.1 by ITU-T for the H.324 and H.323 family of products.

Features

- TrueSpeech at 8.5, 6.3, 5.3, 4.8 and 4.1 kbps at 8KHz sampling rate
- G.723.1 (including Annex A VAD/CNG) and Windows® 95 TrueSpeech 8.5 compatibility
- Real-time Full duplex or Half duplex speech compression and decompression
- Acoustic Echo Cancellation concurrent with TrueSpeech and G.723.1 operation
- Full Duplex Speakerphone
- Host-to-Host (codec-less) and Host-CODEC modes of operation
- Parallel 8-bit host interface provides simple "zero-glue" memory-mapped I/O host connection.
- 1 or 2-channel DMA support (Single Cycle and Burst Modes)
- Flexible A-to-D/D-to-A CODEC interface, low cost PCM μ/A-Law and 16-bit Linear
- CODEC interface supports TDM bus connection
- Automatic handling of frame slippage and frame synchronization
- Automatic AGC for message recording
- Speech level detection and Silence compression
- DTMF and Tone Generation
- DTMF and Programmable Tone Detection
- Pass-through modes - 8-bit and 16-bit linear at 8 KHz and 11 KHz (host programmable codec sample rate)
- Power Down and Power Save modes
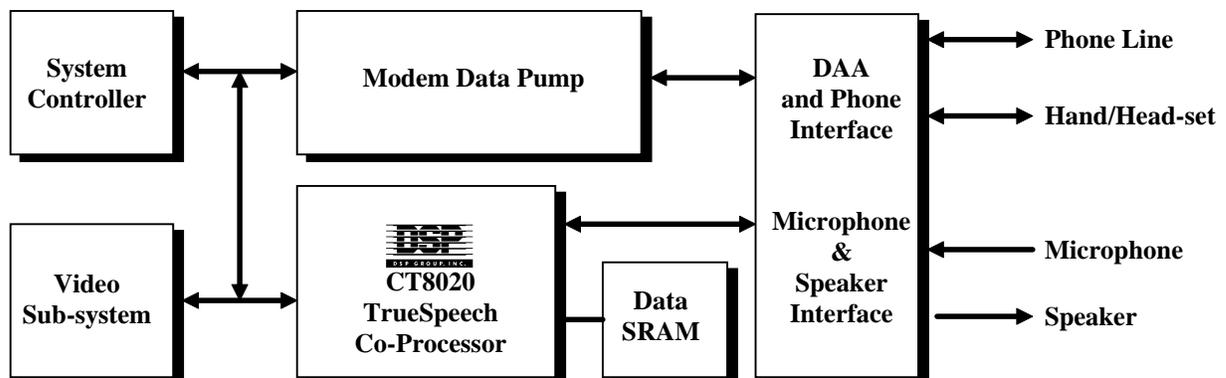

CT8020 System Block Diagram

DSP Group, Inc.

The CT8020, an Application Specific Digital Signal Processor, is controlled by the system's host processor through a simple host interface command protocol. The host processor provides activation and control of all system functions. The CT8020 host interface is capable of full duplex data transfer, aided by variable depth transmit and receive buffers. The host interface supports data transfer using DMA as well as host-interrupt and host-polling modes. The CT8020 supports two modes of uncompressed speech input/output. In HOST-CODEC mode, the uncompressed speech input/output is provided by one of the external serial codecs. In HOST-HOST (codec-less) mode, the Host provides the uncompressed speech input/output via the host interface. In both CODEC and HOST mode, the TrueSpeech compressed speech input/output data is transferred via the host interface.

The only additional external component ICs needed to implement these functions are a low cost 8Kx8 or 32Kx8 SRAM, a CODEC and oscillator crystal circuit.

Note: MOS, Mean Opinion Score is a subjective measure of speech quality where a score of 5 means that the speech quality is Excellent, 4 is Good or Toll Quality (as expected in PSTN) and 3 is fair.

Applications

- Simultaneous Voice and Data Modems
- Teleconferencing and Video Conferencing
- CTI - Computer-Telephony Applications
- Digital Telephony Applications
- Voice Enabled Wireless Terminals

- Real-time compression and de-compression of TrueSpeech 8.5 Windows Sound System and Windows 95 compatible PC speech files
- Store & Forward applications for speech
- Desktop Telephony & Speakerphone

CT8020 Functional Block Diagram

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1. PIN-OUT AND PIN DESCRIPTIONS

Not available electronically at this time. Call (408) 986-4300 and request to have it faxed to your location, or check back shortly.

128 pin PQFP/TQFP

This section contains a list of the CT8020 pins:

Note that the CT8020 is a CMOS device. It is important to make sure that all input pins are connected and have a valid logic level present at all times. Where noted, certain input pins may require external pull-up or pull-down resistors.

Signal naming convention: Active low signals are indicated by a trailing "/" or "N" in the signal name. For example SRAMCS/ or SRAMCSN.

Pin names	Pin Numbers	type	function
HSTDB0 HSTDB1 HSTDB2 HSTDB3 HSTDB4 HSTDB5 HSTDB6 HSTDB7	100 103 104 105 106 109 110 111	I/O/Z	Host Data Bus. HSTDB0 is the least significant data bit.
HSTAB0	112	I	HSTAB0 is the least significant Host Address bit, it selects between the high and low byte of the host interface register selected by HSTAB3-1.
HSTAB1 HSTAB2 HSTAB3	113 114 115	I	Host Address Bus. These address bits are used to select host interface register addressed by host (in conjunction with HSTCS/).
HSTRD/ (HSTRDN)	119	I	Host Read signal. Active Low, output enables HSTDB pins, allowing host to read from the selected host interface register. The interface register is selected via a decode of HSTAB1-3 if HSTCS/ is active, or the Host Receive Data Buffer access port is selected directly if RXDACK/ is asserted.
HSTWR/ (HSTWRN)	120	I	Host Write signal. Active Low, clocks data from HSTDB pins into selected host interface register. The interface register is selected via a decode of HSTAB1-3 if HSTCS/ is active, or the Host Transmit Data Buffer access port is selected directly if TXDACK/ is asserted.
HSTCS/ (HSTCSN)	121	I	Host Interface Chip Select. Active Low. This signal gates the HSTWR/ and HSTRD/ and HSTAB3-0 address decode during a host processor access cycle. The HSTAB3-0 signals should be stable and valid when HSTCS/ is asserted. This signal **must not be asserted** during a DMA cycle on the host port. **HSTCS/ must be high when either TXDACK/ or RXDACK/ are asserted (low).**
TXDREQ	124	O	Active High signal. DMA transmit request. This signal is asserted to indicate that the device is ready to accept transmit data. Data can be transferred either by DMA or a host processor access cycle. This signal can be enabled or disabled by the host via the Hardware Control Register. By default, this signal is disabled.
TXDACK/ (TXDACKN)	125	I	Active Low signal. DMA Transmit Acknowledge. This signal is asserted by an external DMA controller on the host port, together with HSTWR/, to clock a byte from

			the HSTDB databus pins into the host interface Transmit Data Buffer Access port. This signal provides direct access to the Host Transmit Data Buffer Access Port, without involving HSTAB0-3 or HSTCS/. If this signal is not used, it should be connected to VCC via a 10K ohm pull-up resistor. **This signal must not be asserted when either RXDACK/ or HSTCS/ are active**.
RXDREQ	126	O	Active High signal. DMA receive request. This signal is asserted to indicate that the device is ready to provide receive data. Data can be transferred either by DMA or a host processor access cycle. This signal can be enabled or disabled by the host via the Hardware Control Register. By default, this signal is disabled.
RXDACK/ (RXDACKN)	127	I	Active Low signal. DMA Receive Acknowledge. This signal is asserted by an external DMA controller on the host port, together with HSTRD/, to accept a receive data byte via the HSTDB databus pins from the host interface Receive Data Buffer Access port. This signal provides direct access to the Host Receive Data Buffer Access Port, without involving HSTAB0-3 or HSTCS/. If this signal is not used, it should be connected to VCC via a 10K ohm pull-up resistor. **This signal must not be asserted when either TXDACK/ or HSTCS/ are active**.
IRQ/ (IRQN)	118	OC	Interrupt Request. Open collector output (requires external pull-up resistor with min value 1K ohm). This signal is asserted to indicate an interrupt request to the host controller.
MDB0 MDB1 MDB2 MDB3 MDB4 MDB5 MDB6 MDB7 MDB8 MDB9 MDB10 MDB11 MDB12 MDB13 MDB14 MDB15	75 76 77 78 81 82 83 84 87 88 89 90 93 94 95 96	I/O/Z	External Memory Data Bus, used to interface to external memory. When the CT8020 is used with external 8-bit wide data SRAM, the SRAM data lines should be connected to the l.s. CT8020 data pins (MDB7-0). The CT8020 supports external data memory configured as 8Kx8 or 4Kx16.
ADDR0 ADDR1 ADDR2 ADDR3 ADDR4 ADDR5 ADDR6 ADDR7	43 44 45 46 49 50 51 52	O/Z	External Memory Address Bus, used to interface to external memory. Note that the CT8020 is a 16-bit device and the address lines indicate access to 16-bit data words. **When the CT8020 is used with external 8-bit wide SRAM, the least significant address line of the SRAM should be connected to the BSEL pin (byte select)**. In this configuration, the SRAM pin A1 connects to the CT8020 pin A0, SRAM pin A2 connects to the CT8020 pin A1...etc.

ADDR8	55		Note that the CT8020 address pins indicate the **16-bit word** address being accessed, the BSEL pin is used to select between the upper and lower bytes within a word when a byte-wide memory is used.
ADDR9	56		
ADDR10	57		
ADDR11	58		
ADDR12	61		
ADDR13	62		
ADDR14	63		
ADDR15	64		
BSEL	40	O/Z	Byte Select. Used to select the low or high byte accessed during an 8-bit external data access cycle. Driven low to select the low byte. Driven high to select the high byte. **When the CT8020 is used with external 8-bit wide SRAM, the BSEL signal should be used to drive the SRAM A0 pin.** The SRAM A1 pin should be connected to the CT8020 A0 pin, the SRAM A2 pin should be connected to the CT8020 A1 pin ....etc. The state of this pin is defined only during an external data cycle in 8-bit mode. At other times, this pin may be high or low.
DATARD/ (DATARDN)	69	O/Z	External Data Memory Read. Active Low, used to indicate a read cycle from external data memory
DATAWR/ (DATAWRN)	70	O/Z	External Data Memory Write. Active Low, used to indicate a write cycle to external data memory.
PREAD/	65	O/Z	Reserved - NC (do not connect)
PWRITE/	66	O/Z	Reserved - NC (do not connect)
BOOTRD/	72	O/Z	Reserved - NC (do not connect)
SRAMCS/ (SRAMCSN)	71	O/Z	external data SRAM chip select. Active low. This signal is asserted during external data access.
RESET/ (RESETN)	11	I	Reset signal. Active Low, the pin is driven low to reset the device. **Note - this pin is not a TTL input.** VIH = 4.25 volts max. VIL = 1.3 volts min.
GPIO0, DATAFLAG\	1	I/O	General purpose Input/Output pins. for CT8015 compatibility: GPIO 0 may be assigned as DATAFLAG/ (output) GPIO 5 may be assigned as Frame Interrupt, FR/ (output)
GPIO1	2		
GPIO2	3		
GPIO3	4		During reset, the GPIO pins are all configured as inputs.
GPIO4	5		
GPIO5, FR\	6		**Connect 47K ohm pull-down resistors to GND on each GPIO pin to ensure that a valid input signal level is present at all times**.
GPIO6	9		
GPIO7	10		
SCLK	31	I/O	Shift Clock for codec interface. During and after reset, this pin is configured as an input. **Connect 47K ohm pull-down resistors to GND to this pin to ensure that a valid input signal level is present at all times.** If this pin is permanently driven by an external signal, no pull-down is required. The SCLK signal is typically expected to operate at 2.048 MHz. When used as an output (master mode) the SCLK rate is programmable by the

			host.
FSYNC	32	I/O	Frame Sync clock for codec interface. During and after reset, this pin is configured as an input. **Connect 47K ohm pull-down resistors to GND to this pin to ensure that a valid input signal level is present at all times.** If this pin is permanently driven by an external signal, no pull-down is required. The FSYNC signal is typically expected to operate at 8 KHz to provide the 8KHz sample clock required by the external serial codec. When used as an output (master mode), the FSYNC rate is programmable by the host.
DX0	27	O/Z	Serial Transmit Data Output for codec 0. This output is always high impedance when not transmitting data. This codec pin is used for telephone line output in Standalone Speakerphone mode.
DR0	28	I	Serial Receive Data Input for codec 0. **Connect 47K ohm pull-down resistors to GND to this pin to ensure that a valid input signal level is present at all times.** Note that codec chip output pins typically tri-state when not actually transmitting data. This codec pin is used for telephone line input in Standalone Speakerphone mode.
DX1	29	O/Z	Serial Transmit Data Output for codec 1. This output is always high impedance when not transmitting data. This is the default codec output used for playback.
DR1	30	I	Serial Receive Data Input for codec 1 **Connect 47K ohm pull-down resistors to GND to this pin to ensure that a valid input signal level is present at all times.** Note that codec chip output pins typically tri-state when not actually transmitting data. This is the default codec input used for record.
XIN	19	I	Crystal Input or external oscillator input.
XOUT	20	O	Crystal Output
CLKOUT	14	O	Clock Out = MAINCLOCK/(CLK_RATE+1). This is the internal CT8020 DSP core clock. The output may be disabled to reduce power consumption. The MAINCLOCK frequency in PLL mode, is the external crystal frequency * 10. In PLL by-pass mode, MAINCLOCK is the external oscillator frequency divided by 2. See section 9.23.4 for definition of CLK_RATE.
TEST	12	I	Reserved - connect to GND.
PLLR PLLC PLLT	21 22 23	Analog Analog Analog	PLL support circuitry pins. Connect to external PLL filter circuit.
AVCC3	18	I	PLL VCC connection
AGND3	24	I	PLL GND connection
PLLBYPASS	15	I	Disables internal PLL when high and allows direct use of an external (80 MHz) clock applied to the XIN pin. Connect to GND when operating using PLL and external 4 MHz crystal.
BUSREQ/	98	I	Reserved input, active low. Connect this pin to VCC via a 10K ohm pull-up resistor.

BUSGRANT/	99	O	Reserved - NC (**do not connect**)
EXTP	39	I	Reserved - connect to GND
BOOTMODE	128	I	Reserved - connect to GND
DBG	35	I	Reserved - connect to GND
ABORT/	33	I	Reserved, active low - connect to VCC via 10 Kohm pull-up resistor.
BOOT	34	I	Reserved - connect to GND
URST	38	I	Reserved - connect to GND
EXTINT/	13	I	Reserved, active low - connect to VCC via 10 Kohm pull-up resistor.
GND1 GND2 GND4 GND5 GND6 GND7 GND8 GND9 GND10 GND11 GND12 GND13 GND14 GND15 GND16 GND17 GND18	8 17 26 37 42 48 54 60 68 74 80 86 92 102 108 117 123	I	Ground pins
VCC1 VCC2 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18	7 16 25 36 41 47 53 59 67 73 79 85 91 101 107 116 122	I	Power Supply pins
Unused	97		This pin has no internal connection to the device. It may be left un-connected.

Note, pins marked "Reserved - NC (no connect)" should be left un-connected. These Reserved pins are outputs, connecting them to either GND or VCC may cause damage to the device. Other pins are marked either "Reserved - connect to GND" or "Reserved - connect to VCC via 10 K ohm pull-up resistor". These Reserved pins are inputs which require a defined input signal level. They should not be left to "float". Pins

marked as Reserved are not intended for active use by the user. However these pins may be used by other devices in the CT8000 series family.

2. External Component Connections

2.1 PLL Circuit

VCC

100

PLL VCC — AVCC3

XIN

1M — XOUT

1K   100 — PLLR

0.1 uF

Crystal — PLLC

1 nF

+

10 uF

10 pF — PLLT

10 pF   PLL GND — AGND3

PLLBYPASS

Connect to GND at single point

GND
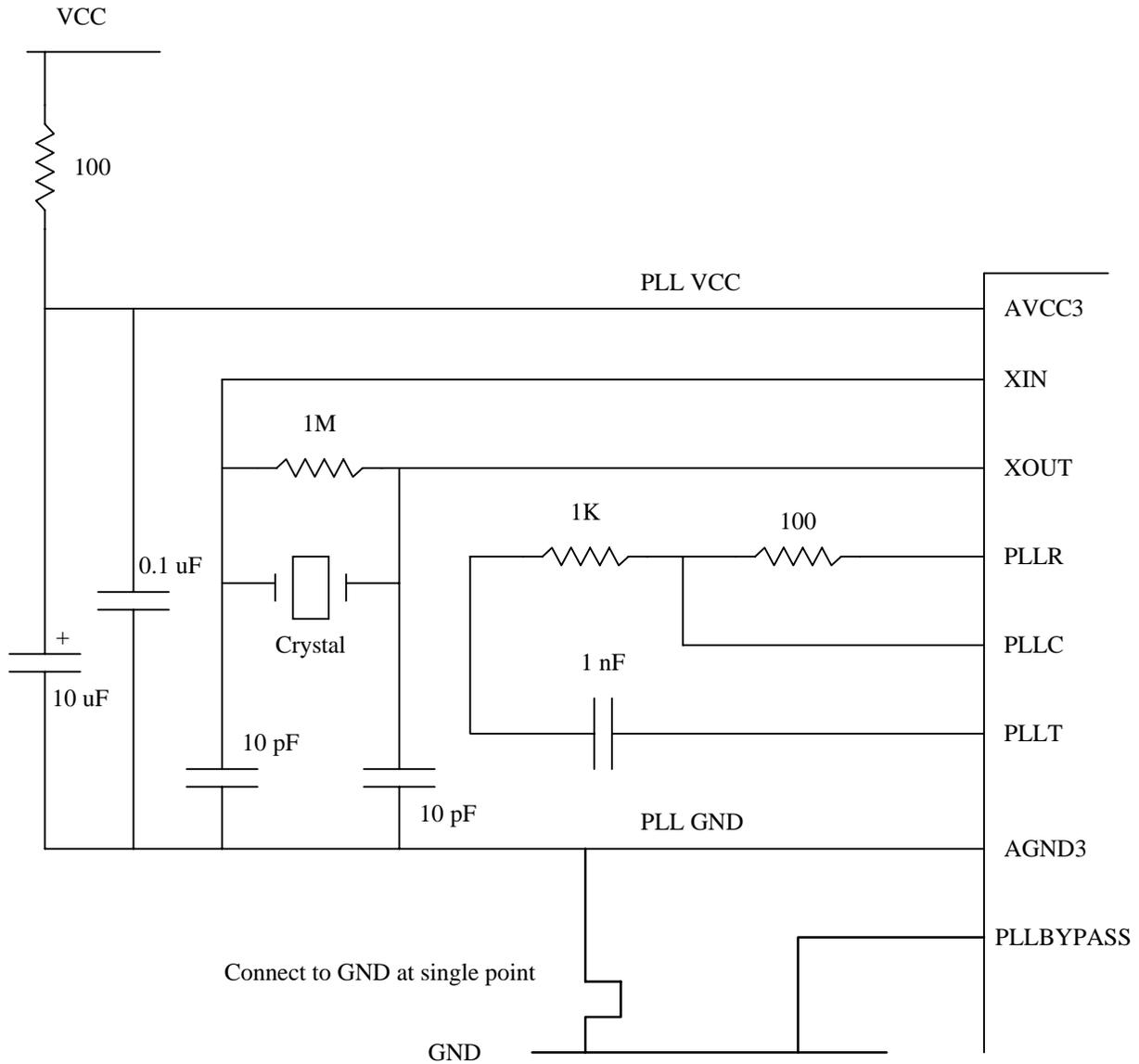
Crystal frequency is nominal 4 MHz. Crystal may be replaced by external 4MHz clock source.

Figure 2-1 PLL Circuit

2.2 CT8020 8-bit external data SRAM connection

```
 _____                                            _____
|DATARD  |————————————————————————————————————————|RD      |
|        |                                          |        |
|DATAWR  |————————————————————————————————————————|WR      |
|        |                                          |        |
|SRAMCS  |————————————————————————————————————————|CS      |
|        |                                          |        |
|ADDR13  |· · · · · · · · · · · · · · · · · · · · · |A14     |
|        |            for 32K x 8 sram only         |        |
|ADDR12  |· · · · · · · · · · · · · · · · · · · · · |A13     |
|        |                                          |        |
|ADDR11  |————————————————————————————————————————|A12     |
|ADDR10  |————————————————————————————————————————|A11     |
|ADDR09  |————————————————————————————————————————|A10     |
|ADDR08  |————————————————————————————————————————|A09     |
|ADDR07  |————————————————————————————————————————|A08     |
|ADDR06  |————————————————————————————————————————|A07     |
|ADDR05  |————————————————————————————————————————|A06     |
|ADDR04  |————————————————————————————————————————|A05     |
|ADDR03  |————————————————————————————————————————|A04     |
|ADDR02  |————————————————————————————————————————|A03     |
|ADDR01  |————————————————————————————————————————|A02     |
|ADDR00  |————————————————————————————————————————|A01     |
|        |                                          |        |
|BSEL    |————————————————————————————————————————|A00     |
|        |                                          |        |
|        |                                          |        |
|MDB07   |————————————————————————————————————————|D7      |
|MDB06   |————————————————————————————————————————|D6      |
|MDB05   |————————————————————————————————————————|D5      |
|MDB04   |————————————————————————————————————————|D4      |
|MDB03   |————————————————————————————————————————|D3      |
|MDB02   |————————————————————————————————————————|D2      |
|MDB01   |————————————————————————————————————————|D1      |
|MDB00   |————————————————————————————————————————|D0      |
|_____|                                          |_____|

   CT8020                                             8K x 8
                                                      SRAM
                                                      25 ns
```
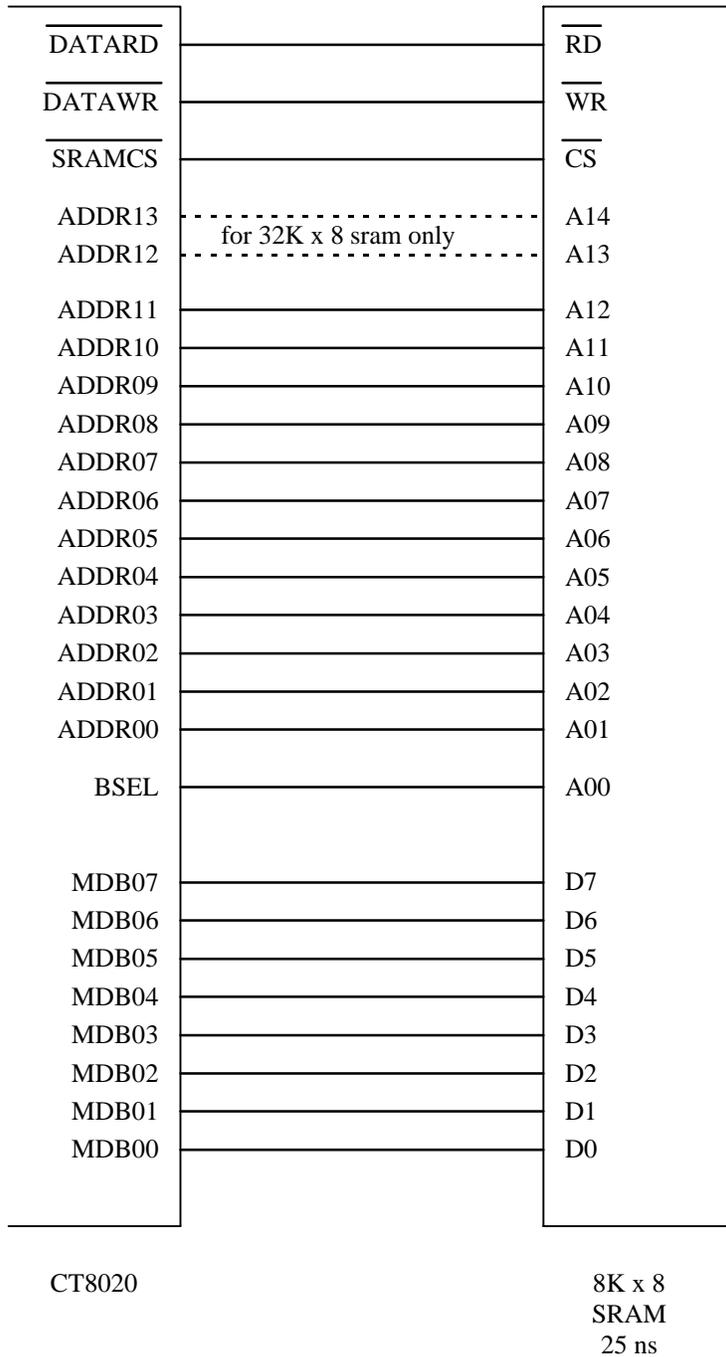
Note that the CT8020 BSEL pin is used to drive the SRAM A0
address line. The CT8020 requires only a 8Kx8 SRAM, but a
32Kx8 SRAM may be used as an alternative.

Figure 2-2 External SRAM connection

2.3 Codec Connection
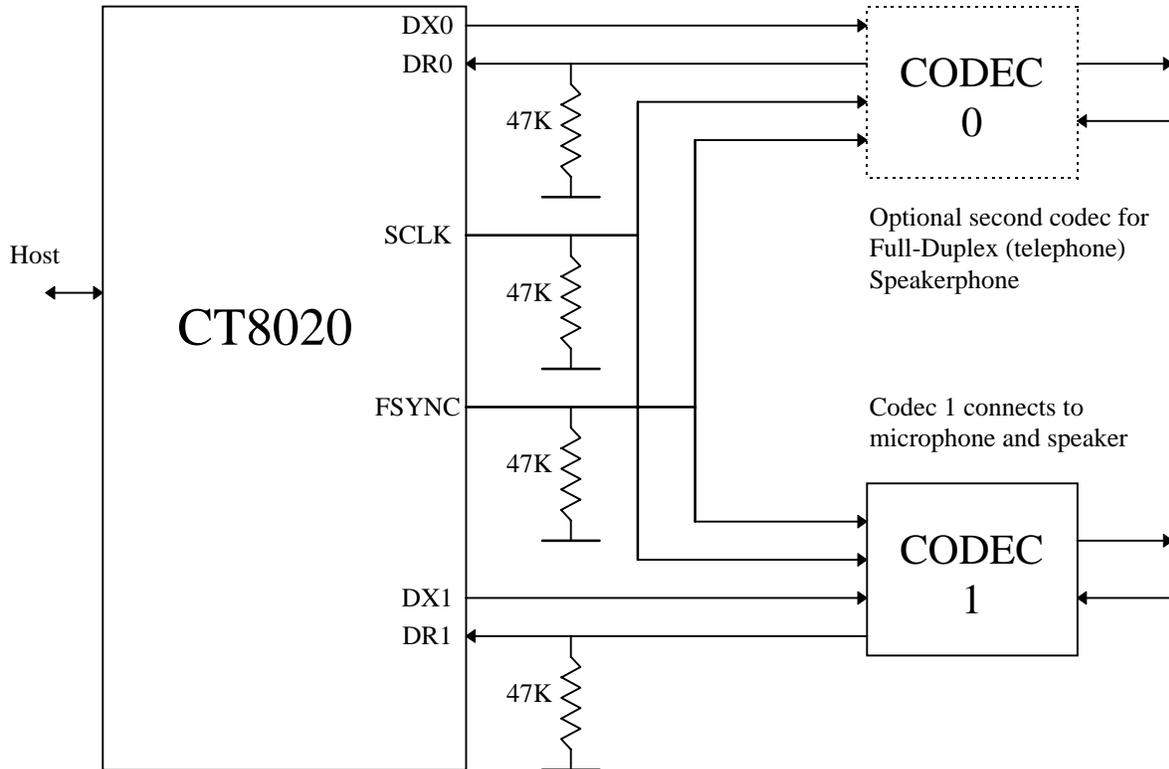
Figure 2-3 CODEC connection

In Master mode, the CT8020 generates the FSYNC and SCLK signals.

In Slave mode, the FSYNC and SCLK signals are generated externally. In slave mode, the CT8020 FSYNC and SCLK pins are inputs.

Note that during and after reset, the SCLK and FSYNC pins are configured as inputs. As such, they require external pull-down resistors to ensure that a safe and defined logic level is present.

CODEC 0 is required only if "Standalone" Full Duplex Speakerphone operation is desired (e.g for use as an analog phone line speakerphone). In this configuration, CODEC 0 connects to the audio input/output of an analog telephone line. CODEC 0 is not required for DSVD/Video Conferencing Speakerphone operation.

For codec-less operation, both CODEC 0 and CODEC 1 may be omitted. In this case, the FSYNC, SCLK, DR0 and DR1 inputs should have pull-down resistors connected to ground to ensure a valid input signal level.

3. FEATURE OVERVIEW

3.1 Introduction

The CT8020 is a full duplex TrueSpeech real-time speech compression Encoder/Decoder. It is designed to operate in conjunction with a host processor and one or two external A-to-D/D-to-A serial CODECs. The host processor is responsible for managing the bi-directional stream of compressed speech data provided by the CT8020. The CT8020 accepts un-compressed speech in 8-bit A-law/mu-law or 16-bit Linear formats at 64/128 Kbits/sec from the receive channel of the external serial CODEC and compresses the speech to TrueSpeech at 8.5, 6.3, 5.3, 4.8 or 4.1 Kbits/sec. The compressed speech is passed to the host processor in frames every 30 ms. At the same time that the CT8020 is compressing speech, it can concurrently accept compressed speech from the host for decompression, outputting the uncompressed speech to the transmit channel of the external codec. The CT8020 supports independent and asynchronous operation of the host receive and transmit (compressed) data streams. The transmit and receive interfaces to the external codec operate synchronously. The device contains variable length buffers for each data direction and also provides support of frame deletion and insertion to accommodate sample clock differences between the source and destination devices.

3.2 Speech Modes

The CT8020 playback (transmit) and record (receive) channels can operate in several different speech modes : TrueSpeech (compressed), A-law/Mu-law (non-compressed), 8-bit and 16-bit linear. In TrueSpeech mode, speech data is exchanged with the host in compressed form, in appropriate sized frames every 30ms. In A-law/Mu-law or 8-bit linear mode, speech data is exchanged with the host in non-compressed mode in frames of 120 words (240 bytes) of A-law/Mu-law or linear data every 30 ms. In this mode, the data rate is 64,000 bits/sec. In 16-bit mode, the data frame size is 240 words (480 bytes). In this mode, the data rate is 128 Kbits/sec. The mode of operation of the playback and record channel can be selected independently of each other.

3.3 TrueSpeech

TrueSpeech is a speech compression technology which reduces or compresses the amount of data used to encode a speech waveform. TrueSpeech compression reduces speech sampled (digitized) at 8,000 samples per second, in 16-bit samples (128,000 bits/sec) to 8.5, 6.3, 5.3, 4.8 or 4.1 Kbits/sec with minimal degradation in speech quality.

In the CT8020, uncompressed speech is obtained from an external codec operating at 8,000 samples per second. If an external A-law or Mu-law codec is used, the speech is sampled by the external codec with 14-bits of resolution. The codec converts the 14-bits (linear) samples to 8-bit A-law/Mu-law for transmission to the CT8020 (at 64,000 bits/sec). The CT8020 receives the speech samples from the codec and converts them back to 14-bit linear form. The 14-bit data is converted to 16 bits by appending two zero bits in the least significant bit positions. The 16-bit data is collected into blocks of 240 samples (480 byte) every 30 ms and TrueSpeech compressed for transfer to the host. If an external linear 16-bit codec is used, the speech data is sampled with 16-bit resolution and passed directly from the CODEC to the CT8020 at 128,000 bits/sec.

The CT8020 supports simultaneous compression and decompression of TrueSpeech data in real-time.

3.4 TrueSpeech 8.5

In TrueSpeech 8.5 mode, speech data is compressed/decompressed into 16-word (32 byte) blocks, which are transferred to or from the host every 30 ms. This corresponds to a data rate of 8,533.33 bits/sec. The CT8020 TrueSpeech 8.5 implementation is compatible with the TrueSpeech 8.5 format used in the CT8005 TrueSpeech Messaging Co-Processor, CT8015 TrueSpeech DSVD Co-Processor and Microsoft Windows Sound System 2.0 and Windows 95 software TrueSpeech CODECs.

3.5 TrueSpeech 6.3 (G.723.1)

The CT8020D11AQC version of the CT8020 implements the final (version 5.1) ITU-T formal release of the G.723.1 speech coder standard, including G.723.1 Annex A.

In TrueSpeech 6.3 (G.723.1), data is compressed into 12-word blocks. This provides 192 bits per block. However, only 189 bits are used for actual speech data, giving a raw data rate of 6,300 bits/sec. When used in compliance with G.723.1 two of the spare bits are assigned for control information. The CT8020 G.723.1 implementation includes the optional G.723.1 Annex A VAD/CNG "silence" compression feature (Voice Activity Detection / Comfort Noise Generation). When this feature is enabled, the CT8020 can generate and decode the 4-byte and 1-byte Annex A silence frames. The CT8020 supports dynamic switching between the G.723.1 6.3 and 5.3 rates for both the encoder and decoder. In addition, the G.723.1 6.3 and 5.3 decoders support frame erasure (for corrupt or missing frames) using specially marked data frames.

3.6 TrueSpeech 5.3 (G.723.1)

In TrueSpeech 5.3, data is compressed into 10-word blocks. This provides 160 bits per block. However, only 158 bits per block are used for actual speech data, giving a raw data rate of 5,266.67 bits/sec. When used in compliance with G.723.1, the two "spare" bits are used for control information. The 5.3 rate can be operated in conjunction with the VAD/CNG silence compression feature.

3.7 TrueSpeech 4.8

In TrueSpeech 4.8, data is compressed into 9-word blocks. This provides 144 bits per block. However only 142 bits per block are used for actual speech data, giving a raw data rate of 4733.33 bits/sec. The 4.8 rate can be operated in conjunction with the VAD/CNG silence compression feature.

3.8 TrueSpeech 4.1

In TrueSpeech 4.1, data is compressed into 8-word blocks. This provides 128 bits per block. However only 124 bits per block are used for actual speech data, giving a raw data rate of 4133.33 bits/sec. The 4.1 rate can be operated in conjunction with the VAD/CNG silence compression feature.

3.9 Automatic Gain Control

In speech record mode (compressed or uncompressed), the CT8020 record process can optionally include an Automatic Gain Control (AGC) function. When this feature is enabled, the CT8020 can automatically adjust the record signal level by internal digital scaling of the input speech signal. The control parameters for the AGC, which include max and min gain (amplification), attack and decay times (response time) are

programmable by the host. Note that for optimal AEC performance in DSVD mode, use of the AGC feature concurrently with the Acoustic Echo Canceller is not recommended. However, where the user considers simultaneous use of both AEC and AGC to be necessary, the CT8020 does include a mechanism to reduce the echo amplification effect caused when the AGC gain increases.

3.10 Record and Playback Volume

The CT8020 supports host programmable record and playback volume controls. This enables internal digital scaling of the input and output speech signal levels. The host can elect to use fixed level settings during record in situations where AGC operation is not desired (for example - high noise environments). Also AGC operation is not appropriate in full duplex speech mode when the Acoustical Echo Cancellor (AEC) is active, since the AGC would interfere with the ability of the AEC to operate correctly. In particular, the AGC would operate to amplify the canceled (attenuated) echo signal.

3.11 DSVD

Digital Simultaneous Voice and Data is a protocol used to enable collaborative computing where voice conversation and full duplex data transfers occur simultaneously over a single telephone line via a high speed modem. Since the data transfer rate achievable over a telephone line is limited, speech compression is required to make it possible to send speech simultaneously with data. Applications for DSVD include application sharing, shared whiteboard and interactive games.

3.12 Microsoft Windows® Sound System

In addition to supporting playback and recording of compressed TrueSpeech data, the CT8020 can also playback and record un-compressed data in 16-bit linear, 8-bit linear, 8-bit mu-law and 8-bit A-law formats. The 8-bit linear format supports data in both signed and unsigned form (with or without most significant data bit inversion). This provides true Windows Sound System (WSS) 8 bit .wav file compatibility. The CT8020 supports 8- and 16-bit 8 KHz, and 11 KHz Microsoft WAVE file mono formats making it an ideal low cost device for speech enabling personal computers and personal digital assistants (PDAs). The Microsoft WAVE file format also includes support for storing of TrueSpeech 8.5 speech data, making it possible to directly exchange TrueSpeech WAVE recordings with WSS compliant PC's. A "software only" TrueSpeech 8.5 encoder/decoder is a standard part of the Sound Recorder application included with Windows® 95.

3.13 Data Compression/De-Compression Accelerator

The CT8020 can be used a data compression accelerator. In addition to supporting real-time recording and playback via external CODECs, the CT8020 can operate in a codec-less environment where it compresses 16-bit linear speech data from the host, returning the compressed data to the host. Simultaneous compression and decompression is supported. This enables the CT8020 to be used in a sound-card type environment where the speech input and output channels are independent of the CT8020.

3.14 DTMF / Tone Generator

The DTMF/Tone generator can generate any single or dual frequency tone in the range 300Hz to 3 KHz. The CT8020 has preset parameters for generating all 16 DTMF digits (0-9, *, #, and the "hidden" digits A, B, C, D) as well as standard USA dial tone, busy tone, and ringing (ringback) tone. The preset parameters

can be re-programmed by the host controller to generate any single or dual frequency tone combination. The relative level (twist) of dual frequency tones can also be selected.

3.15 Tone Detection

The CT8020 contains a set of four independent programmable call progress tone filters which can be used to detect call progress tones such as dial tone, busy tone, ringing (or ringback) tone and fax calling tone (CNG).

3.16 DTMF Detection

The CT8020 includes a DTMF detector which can detect all 16 DTMF digits including the digits ABCD.

3.17 Full Duplex Speakerphone

The CT8020 can operate in either **Standalone** Speakerphone or in **DSVD** Speakerphone mode. In DSVD Speakerphone mode, the CT8020 provides Acoustical Echo Cancellation between the speaker and microphone connection concurrent with TrueSpeech operation. In Standalone Full duplex Speakerphone mode, Acoustical Echo Cancellation as well as near-end (Electrical) echo cancellation to the telephone line connection are provided. Standalone Speakerphone mode provides support for creating an analog phone line based speakerphone.

Unlike many Speakerphone implementations, the CT8020 implements a **Full Duplex Speakerphone.** In most speakerphones, only one party can talk at once, the other party is always muted, sometimes by as much as 50 dB or more. This is **Half Duplex Speakerphone** operation. In half-duplex operation a Speakerphone "listens" to both the microphone and the telephone line inputs and tries to detect which direction is talking. It allows input from the talking direction and mutes input from the other direction. If this were not done, acoustical feedback or "howling" would take place. The major problem with a half-duplex Speakerphone is that a user experiences "break up" in the conversation when the Speakerphone incorrectly identifies the talking party (due to noise) or both parties attempt to talk at the same time.

The CT8020 implements a Full Duplex Speakerphone. This implementation allows both parties to speak at once and be heard by the party at the opposite end of the call. It does this using DSP technology called acoustical echo cancellation. Acoustical echoing occurs when the Speakerphone microphone picks up the audio signal from the Speakerphone speaker ,"echoing" the output (speaker) signal back along the telephone line. The signal sent down the telephone line is also "echoed" by the telephone line and re-output to the speaker. This creates a "feedback" loop : the signal from the phone line is output from the speaker, picked up by the microphone, sent to the phone line, echoed by the phone line and re-output by the speaker. This causes "howling" or "howl round", a loud annoying high pitched noise. In the CT8020, "howling" is prevented by the use of echo cancellation. This is an adaptive filtering process where the CT8020 compensates for the speaker-to-microphone echo and subtracts the outgoing speaker signal from the incoming microphone signal reducing or eliminating the acoustic echo.

See Appendix A for more details on speaker phone operation

3.18 Acoustical Echo Cancellation

The CT8020 includes an Acoustical Echo Cancellor (AEC) as part of its Full Duplex Speaker phone feature. In addition to its use in standalone speakerphone mode, the AEC can be operated concurrently with the CT8020 full duplex speech mode (DSVD mode). This enables the CT8020 to provide acoustic echo

cancellation between the speaker and microphone while simultaneously providing full duplex speech compression/decompression. This makes possible "hands free" DSVD (DSVD or Video Conferencing Speakerphone) applications avoiding use of a headset or handset for speech input/output. The AEC implementation included in the CT8020D11AQC chip revision contains features that allow the echo cancellor to be used to cancel non-acoustical echoes, for example the electrical signal echo from a 2-to-4 wire telephone hybrid. This option supports use of the CT8020 in a digital speech telephony gateway type application.

3.19 8 / 16 bit host controller interface

The operation of the CT8020 is controlled via 8 16-bit registers which provide a control/status/data interface. This interface is accessed physically as 16 8-bit wide I/O locations mapped into the host controller address space. This allows the CT8020 to be used with inexpensive 8-bit micro-controllers or more powerful 16/32 bit microprocessors. The host controls the CT8020 by writing control words to the CT8020 registers and it obtains status information by reading the CT8020 status registers. Speech data is passed through the receive/transmit buffer registers when recording or playing speech data to or from the host. Receive and Transmit data buffers are 16 words deep and Host controllable. In addition, CT8020 provides either single cycle or continuous (burst) DMA modes for both half duplex and full duplex speech transfers.

3.20 CODEC Interface

The CT8020 supports direct connection to one or two external 8-bit A-law/mu-law or 16-bit Linear CODECs for input and output of audio signals. If two codecs are used, both codecs must be of the same type. The CT8020 can act either as codec clock master, or be driven by an external codec clock. In master mode the codec clock signals SCLK and FSYNC are generated by integer division from the internal CT8020 clock.

3.21 CT8020 Crystal

The CT8020 includes a clock frequency multiplying PLL (phase-locked-loop) to avoid requiring a high frequency external clock source for generation of the internal 40 MHz CT8020 clock. The PLL allows generation of the main internal 40 MHz DSP core clock from an external 4MHz primary clock or crystal. The PLL circuit also includes a by-pass control pin to allow the direct use of an external 2X (80 MHz) clock source applied to the XIN pin.

If the PLL is enabled, the CT8020 primary 4MHz clock can be provided either by attaching a crystal at XIN/XOUT, or by providing a clock input at XIN from an external oscillator. Operation of the PLL is independent of the nature of the primary clock source. If the PLL is disabled, then clock must be provided by an external 80 MHz clock applied at XIN. The XIN-XOUT internal oscillator is not capable of supporting operation with an 80 MHz crystal.

Selection of the precise CT8020 internal clock frequency may depend on the desired CODEC clock frequency. The CODEC normally requires two clock signals : SCLK and FSYNC. The FSYNC signal determines the CODEC sample rate. For TrueSpeech compatible operation, this clock must be exactly 8.0 KHz. The SCLK signal is used to clock the serial data transfer between the CT8020 and CODEC. It is also often used to control the bandwidth of the anti-aliasing filter within the external CODEC. In a standard telecom A-law or Mu-law codec, a SCLK of 2.048 is specified to achieve an audio bandwidth to 3.4 KHz. If the CT8020 is operated in master mode with a which **requires** a SCLK at **exactly** the 2.048 MHz frequency, the CT8020 internal clock must be 38.912 MHz (3.8912 MHz external crystal). This frequency value is a simple integer multiple (x 19) of 2.048 MHz. However it is usually possible to operate standard A-law or Mu-law codecs with a slightly lower SCLK frequency of 2.0 MHz. For example the Texas

Instruments TP3054 and TP3057. The effect of using a lower frequency SCLK is to slightly reduce the bandwidth of the codec audio input/output. Operating with SCLK at 2.0 MHz allows use of a lower cost, standard value, 4.0 MHz crystal. Note that the AT&T T7525 16-bit linear codec **requires** SCLK to be exactly 2.048 MHz in order to operate with FSYNC at 8.0 KHz.

Independent of specific CODEC considerations, the clock frequency requirements are:
1. The internal CT8020 clock must not exceed 40 MHz (4 MHz external crystal).
2. The FSYNC frequency must be exactly 8.0 KHz (for TrueSpeech operation).
3. The clock rate is fast enough to provide the internal computation speed required by the CT8020 for the desired operations.
4. For 8-bit codecs the SCLK frequency must be at least 16 times the FSYNC frequency.
5. For 16-bit codecs the SCLK frequency must be at least 32 times the FSYNC frequency.

3.22 Power Save Modes

The CT8020 supports internal clock slow down modes where the clock rate to the internal DSP core can be reduced. Operation in a slow down mode affects only the clocks to the CT8020 DSP core. The operation of the codec and host interfaces is not affected by slowing down the DSP core. The CT8020 also has a minimum power mode, where all internal clocks are stopped.

4. HOST CONTROLLER INTERFACE

4.1 8 or 16 bit host controller interface

The operation of the CT8020 is controlled via 8 16-bit registers which provide a control/status/data interface. This interface is accessed physically as 16 8-bit wide I/O locations mapped into the host controller address space. This allows the CT8020 to be used with inexpensive 8 bit micro-controllers or more powerful 16/32 bit microprocessors. The host controls the CT8020 by writing control words to the CT8020 registers and it obtains status information by reading the CT8020 status registers. Speech data is passed through the receive/transmit buffer registers when recording or playing speech data to or from the host. Receive and Transmit data buffers are 16 words deep and Host controllable. In addition, CT8020 provides either single cycle or continuous (burst) DMA modes for both half duplex and full duplex speech transfers.

4.2 Host Interface Signals

HSTRDN   Active low: asserted by the host to read from the CT8020

HSTWRN   Active low: asserted by the host to write to the CT8020

HSTCSN   Active low: Chip Select, asserted by the host to enable the HSTRDN, HSTWRN signals

HSTAB3-0   Host Address lines, select the host interface register read or written

HSTDB7-0   8 bit host data bus to transfer data to/from the CT8020

IRQN   Active low: Dedicated host interrupt request (replaces CT8015 ACK signal)

TXDREQ   TX DMA request (associated with data write buffer)

TXDACKN   Active low: TX DMA acknowledge

RXDREQ   RX DMA request (associated with data read buffer)

RXDACKN   Active low: RX DMA acknowledge

4.3 CT8020 Host Connection with external DMA controller
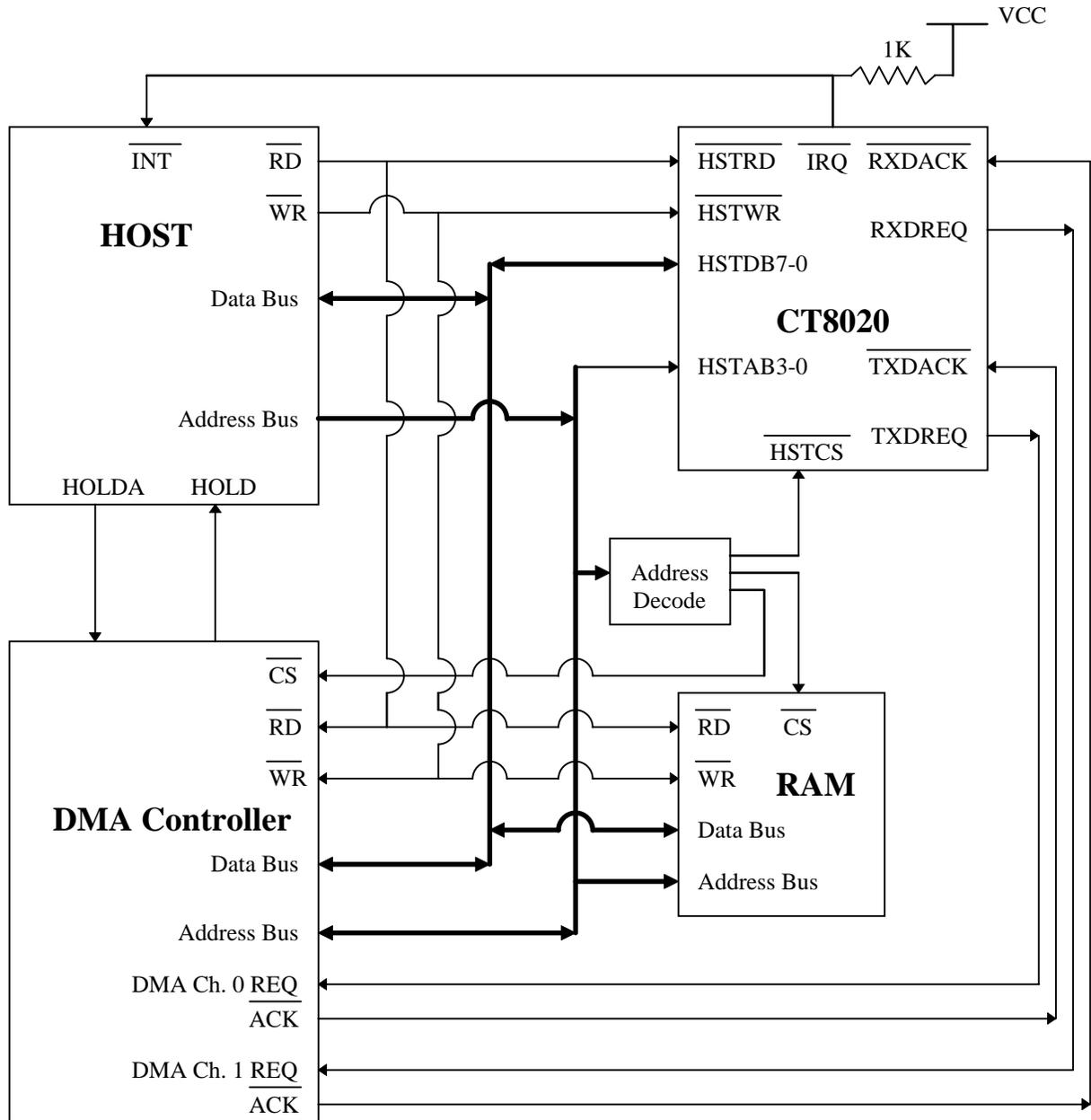
Figure 4-1 CT8020 connection to Host and external DMA controller

4.4 Host Programmers Model

Host Byte Address HSTAB3-0	Host Word Address HSTAB3-1	Function	Access
0-1	0	Aux Software Status Register (Reserved)	Read Only
2-3	1	Software Status Register	Read Only
4-5	2	Aux Software Control Register (Reserved)	Read/Write
6-7	3	Software Control Register	Read/Write
8-9	4	Hardware Status Register	Read Only
A-B	5	Hardware Control Register	Read/Write
C-D	6	Host Transmit (Write) Data Buffer Access Port (buffer input)	Write Only
E-F	7	Host Receive (Read) Data Buffer Access Port (buffer output)	Read Only

Note that the CT8020 registers are all internally 16-bits wide. Physical access to these registers is made using two 8-bit access cycles via the Host Interface. The lower byte of each register is accessed when address line HSTAB0 = 0. The upper byte of each register is accessed when address line HSTAB0 = 1. The registers should always be accessed low byte first followed by high byte. Accesses to the upper byte of the Software Status, Software Control, and Data Buffer Access Port Registers trigger certain internal events within the CT8020. For example reading the upper byte of the Software Status Register clears the Status Ready bit in the Hardware Status Register.

4.5 Register Descriptions

4.5.1 Hardware Control Register

This register has read/write access from the host.

0	0	0	0	0	Host IRQN Master Enable	CONTINUE	DMA Direction
(15)	(14)	(13)	(12)	(11)	(10)	(9)	(8)

TX DMA Burst Mode	RX DMA Burst Mode	TX DMA Enable	RX DMA Enable	Aux Status Update IE	Status Update IE	TX Ready IE	RX Ready IE
(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)

TX DMA Burst Mode	When this bit is set, the TX DMA interface operates in Burst Mode. In Burst Mode, the TXDREQ signal is continuously asserted if the TX Ready bit for the Host Transmit buffer is set. When this bit is clear, the TX DMA interface operates in Single Cycle Mode. In Single Cycle Mode, the TXDREQ signal is de-asserted every time the TXDACKN and HSTWRN signals are asserted, then re-asserted if the TX Ready bit is still set, after a delay (buffer not full). See section on DMA Transfers.
RX DMA Burst Mode	When this bit is set, the RX DMA interface operates in Burst Mode. In Burst Mode, the RXDREQ signal is continuously asserted if the RX Ready bit for the Host Receive buffer is set. When this bit is clear, the RX DMA interface operates in Single Cycle Mode. In Single Cycle Mode, the RXDREQ signal is de-asserted every time the RXDACKN and HSTRDN signals are asserted, then re-asserted if the RX Ready bit for the Host Receive Buffer is still set, after a delay (buffer not empty). See section on DMA Transfers.
DMA Direction:	This field allows the host to use the DMA features in a full duplex or half duplex configuration. In a half-duplex configuration, the host needs to interface a single DMA channel to the CT8020, and needs to be able to transfer data in either direction with this single channel. This is accommodated within the CT8020 by permitting the functional exchange of the external (physical) DMA interface pins. See section on DMA Transfers.
0	Normal Direction. The TXDREQ, RXDREQ, TXDACKN and RXDACKN operate in the manner described in the CT8020 pin out. After reset, this bit is set to zero.
1	Reverse Direction. The physical pin functions of TXDREQ and RXDREQ, and also TXDACKN and RXDACKN are exchanged, i.e. the TXDREQ pin

assumes the function and behavior of the RXDREQ pin and vice-versa. See the section on Half-Duplex DMA mode (page 28) for more information on this feature.

TX DMA Enable :   Setting this bit to 1 enables the TXDREQ and TXDACKN signals. If this bit is set to zero, the TXDACKN signal is ignored and the TXDREQ signal is not asserted. This control operates on the logical TX DMA signals, not the physical pins whose functions can be exchanged between RX and TX.
After reset, this bit is zero.

RX DMA Enable :   Setting this bit to 1 enables the RXDREQ and RXDACKN signals. If this bit is set to zero, the RXDACKN signal is ignored and the RXDREQ signal is not asserted. This control operates on the logical RX DMA signals, not the physical pins whose functions can be exchanged between RX and TX.
After reset, this bit is zero.

HOST IRQN   Setting this bit to 1 enables the IRQN output signal. If this bit is not set the IRQN
Master Enable   signal is not asserted.
After reset, this bit is zero.

Aux Status Update   If this bit is set, the Host IRQN signal is asserted whenever the Aux Status Ready bit
IE   in the Hardware Status Register is set.
After reset, this bit is zero.

Status Update IE   If this bit is set, the Host IRQN signal is asserted whenever the Status Ready bit in the Hardware Status Register is set.
After reset, this bit is zero.

TX Ready IE   If this bit is set, the Host IRQN signal is asserted whenever the TX Ready bit in the Hardware Status Register is set.
After reset, this bit is zero.

RX Ready IE   If this bit is set, the Host IRQN signal is asserted whenever the RX Ready bit in the Hardware Status Register is set.
After reset, this bit is zero.

CONTINUE   The host writes a 1 to this bit to clear the COHOST SHUTDOWN bit in the Hardware Status Register. This returns the host and codec logic to normal operation from sleep mode.
This bit always reads as a 0.
When COHOST SHUTDOWN is in operation, only the continue bit in the Hardware Control Register is accessible. All other bits are undefined for read and write operations.
COHOST SHUTDOWN is a power save state where the CODEC and HOST sections of the CT8020 are disabled in order to reduce power consumption. In this state it is still possible for the CT8020 DSP core to remain active.

4.5.2 Hardware Status Register

This register is read only accessible by the Host.

0	0	0	0	0	COHOST SHUT DOWN	TX DMA	RX DMA
(15)	(14)	(13)	(12)	(11)	(10)	(9)	(8)

IRQN Asserted	SYSTEM RESTART	TX Ready	RX Ready	Aux Status Ready	Status Ready	Aux Control Ready	Control Ready
(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)

SYSTEM RESTART:	reserved
TX Ready:	This bit reflects the state of the TX Ready bit in the DSP's Host Transmit Buffer control register. This bit is set to indicate that the Host Transmit Data Buffer can be accessed by the host. When the host writes to the high byte of the Host Transmit Data Buffer access port and the Frame Size limit is reached (buffer full), this bit is cleared. After reset, this bit is clear. When this bit is set and the TX Ready IE bit in the Hardware Control Register is set, the Host IRQN signal is asserted.
TX DMA:	This bit is set if the (logical) TXDREQ signal is asserted. The state of this bit is affected by the TX DMA enable bit in the host interface hardware control register. If the TX DMA enable is not set, this bit will always be zero.
RX Ready:	This bit reflects the state of the RX Ready bit in the DSP's Host Receive Buffer control register. This bit is set to indicate that the Host Receive Data Buffer can be accessed by the host. When the host reads from the high byte of the Host Receive Buffer access port, and the Frame Size limit is reached (buffer empty), this bit is cleared. After reset, this bit is clear. When this bit is set and the RX Ready IE bit in the Hardware Control Register is set, the Host IRQN signal is asserted.
RX DMA:	This bit is set if the (logical) RXDREQ signal is asserted. The state of this bit is affected by the RX DMA enable bit in the host interface hardware control register. If the RX DMA enable is not set, this bit will always be zero.
Status Ready:	This bit is set when the Oak core writes to the Software Status Register. When the host reads the high byte of the Software Status Register, this bit is cleared. After reset, this bit is cleared. When this bit is set and the Status Ready IE bit in the Hardware Control Register is set, the Host IRQN signal is asserted.

IRQN Asserted:	This bit reflects the state of the external IRQN pin. If the IRQN signal is asserted, this bit is set. If the Host IRQN Master Enable is not set, this bit will always be zero.
Control Ready:	This bit is set when the Oak core reads from the Software Control Register. When the host writes to the high order byte of the Software Control Register, this bit is cleared. After reset, this bit is cleared to indicate that the CT8020 is not ready to receive commands. Once the CT8020 is ready to begin communication with the host, it performs a dummy read of the Software Control Register to set the Control Ready bit.
Aux Status Ready:	This bit is set when the Oak core writes to the Aux Software Status Register. When the host reads the high byte of the Aux Software Status Register, this bit is cleared. After reset, this bit is cleared. When this bit is set and the Aux Status Ready IE bit in the Hardware Control Register is set, the Host IRQN signal is asserted.
Aux Control Ready:	This bit is set when the Oak core reads from the Aux Software Control Register. When the host writes to the high order byte of the Aux Software Control Register, this bit is cleared. After reset, this bit is cleared to indicate that the CT8020 is not ready to receive commands. Once the CT8020 is ready to begin communication with the host, it performs a dummy read of the Aux Software Control Register to set the Aux Control Ready bit.
COHOST SHUTDOWN	This bit indicates that the codec and host interface logic is in sleep mode (power save). The host interface must be re-awakened by writing to the CONTINUE bit in the Hardware Control Register before writing or reading from any other host register. When COHOST SHUTDOWN is active, all the other bits in the Hardware Status Register are undefined for read operations.

4.5.3 Software Control Register

These is a 16-bit register. It is used to pass commands from the host to the CT8020. The host can write commands into this register and also read back the command after it has been written.

When the host writes to the upper byte of one of this register, it clears the Control Ready bit in the Hardware Status Register.

When the CT8020 internally reads from this register, it sets the Control Ready bit in the Hardware Status Register.

The CT8020 hardware includes a second "Aux Software Control Register". This register is reserved and is not used by the internal CT8020 firmware.

4.5.4 Software Status Register

This is a 16-bit register. It is used to pass command status/result information from the CT8020 back to the host. The host can only read from this register.

When the CT8020 updates this register, it sets the Status Ready bit in the Hardware Status Register and also asserts IRQN to the host (if enabled).

When the host reads the upper byte of one of this register, it clears the Status Ready Hardware Status Register. The IRQN will also clear at this time, if enabled.

The CT8020 hardware includes a second "Aux Software Status Register". This register is reserved and is not used by the internal CT8020 firmware.

4.5.5 Host Receive and Transmit Data Buffer Blocks

The CT8020 includes **two** 16-word (32 byte) data buffer blocks for use in transferring blocks of data to or from the host. Access to these buffers is controlled by the CT8020. The host accesses these buffers in sequential address order through two 16-bit Host Data Buffer access ports (one for RX and one for TX). The host address sequence is generated by an internal address counter within the CT8020.

Each buffer is shared between the Host and CT8020. At any one time, either the Host or the CT8020 has access to the buffer, at no time can both Host and CT8020 access the buffer simultaneously. The CT8020 controls whether access belongs to the CT8020 or Host via an internal control register. For example, when the host transmits data to the CT8020, the CT8020 first grants the host access to the buffer. The host fills the "empty" buffer. While the host is filling the buffer, the CT8020 can not access it. Once the buffer is full, the CT8020 regains access to the "full" buffer. The CT8020 then copies the data from the buffer. At this point the host can not access the buffer. Once the buffer has been emptied, the CT8020 can then pass it back to the host.

The receive and transmit buffer blocks are conceptually almost identical except for the direction of data transfer associated with host accesses. The Receive buffer is used to transfer data from the CT8020 to the host. The Transmit buffer is used to transfer data from the host to the CT8020.

Host Receive Data Buffer Block

This block is used to transfer data from the CT8020 to the host, using an external DMA controller or a host processor access cycle.
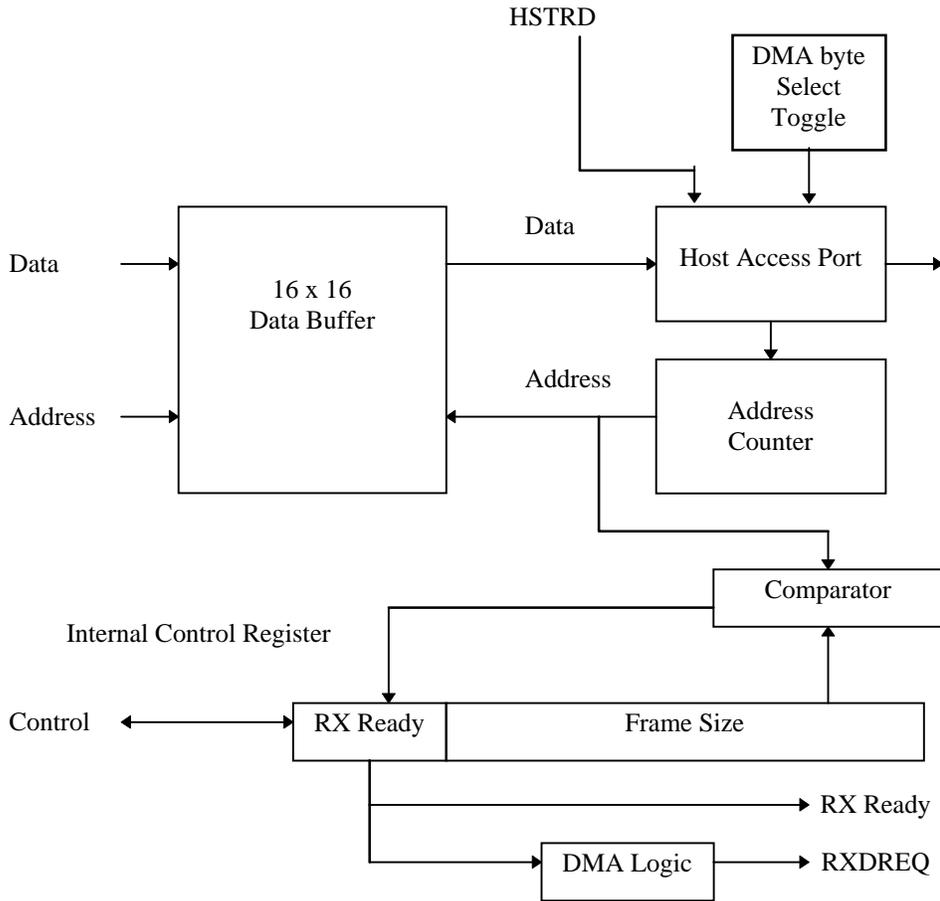
Figure 4-2 Host Receive Data Buffer Block

RECEIVE DATA BUFFER INTERNAL CONTROL REGISTER

0000 0000	RX Ready	00	Frame Size
(15-8)	(7)	(6-5)	(4-0)

This is an internal register, and is not accessible by the host.

RX Ready   When set to zero, the CT8020 has control of the data buffer and has write only access to any location in the buffer.

When set to one, the host has control of the data buffer and may read its contents via the Host Data Buffer access port.

The state of this bit can be checked by the Host at any time since it is reflected by the RX Ready bit in the Hardware Status register. The RX Ready bit in the Receive Data Buffer Control Register drives the RX Ready bit and also RXDREQ via the DMA logic.

After reset, this bit is zero.

Frame Size   The Frame Size field determines the number of words contained in the data buffer. It acts as the reference input to the host buffer address comparator.

ADDRESS COUNTER

The 5-bit address counter provides the sequential buffer access address for access by the host via the Host Data Buffer access port. The address counter is reset to zero when the CT8020 writes a 1 to the RX Ready bit of the internal control register causing control of the buffer to transfer to the Host. Each time the host accesses the upper byte of the Host Data Buffer access port the address counter increments by 1.

The data buffer access port is only physically 8-bits wide. When an access to this port is made by a host processor, the byte select address line HSTAB0 is valid and can be used to select the byte accessed. When access is made by a DMA controller, the address decode which selects the data buffer access port is provided by the RXDACKN signal. During a DMA cycle, the HSTAB3-0 address bits are not valid. Generation of an internal HSTAB0 is thus required to select the byte accessed. This is provided by a simple toggle mechanism which changes state on each DMA access. The DMA byte select toggle is set to zero each time the RX Ready bit changes from a zero to a one (this also clears the main address counter). A separate DMA byte select toggle is required for transmit and receive.

COMPARATOR

The 5-bit comparator is active only when the Host has control (the RX Ready bit is set). The comparator compares the value in the address counter with the value in the Frame Size field. If the values are not equal, the host continues to have access to the data buffer. When the values become equal (after the last host access), the RX Ready bit is reset, transferring control back to the CT8020.

TRANSFERRING DATA FROM CT8020 TO HOST

The CT8020 determines the size of the data frame to be transferred by some protocol with the Host. At the beginning of data transfer, the RX Ready bit will be zero. The CT8020 then writes the appropriate number of words into the data buffer. It then programs the Frame Size and sets the RX Ready bit. This causes the RX Ready bit visible to the Host n the Hardware Status Register to be set. The host discovers that the RX Ready bit is set (by polling or interrupt). The Host then reads Frame Size words from the Host Receive Buffer Access Port, after each word is read, the address counter increments. When the host reads the last word, the address counter is incremented and matches the Frame Size value. This is detected by the comparator which causes the RX Ready bit to be cleared. The CT8020 determines that it has access to the data buffer and loads the next frame into the buffer. This process is repeated to transfer the next frame.

For DMA transfers, the RX Ready bit drives the state of the DMA Request signal. When RX Ready is set, the DMA request is asserted. When the buffer becomes empty, and buffer control automatically returns to the CT8020, the RX Ready bit is cleared and the DMA Request signal is de-asserted.

Host Transmit Data Buffer Block

This block is used to transfer data from the host to the CT8020, using an external DMA controller or a host processor access cycle.
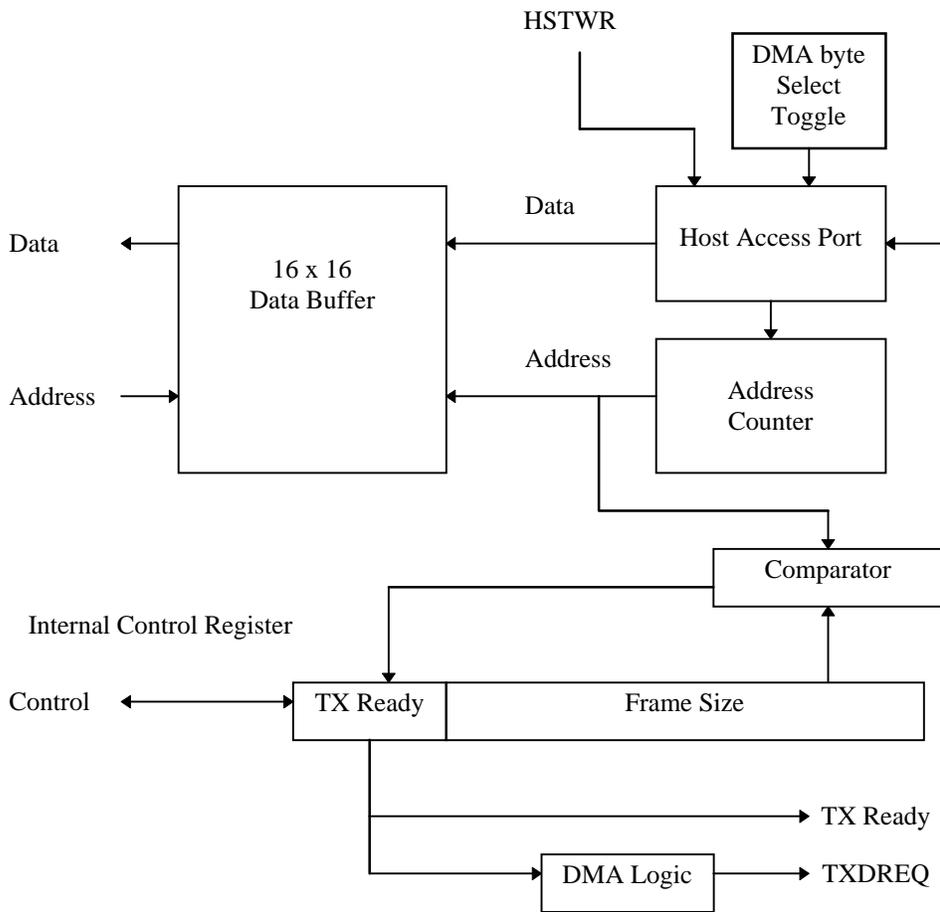
Figure 4-3 Host Transmit Data Buffer Block

TRANSMIT DATA BUFFER INTERNAL CONTROL REGISTER

0000 0000	TX Ready	00	Frame Size
(15-8)	(7)	(6-5)	(4-0)

This is an internal register, and is not accessible by the host.

TX Ready   When set to zero, the CT8020 has control of the data buffer and can read any location in the buffer.

When set to one, the host has control of the data buffer and may write its contents via the Host Data Buffer access port.

The state of this bit can be checked by the Host at any time since it is reflected by the TX Ready bit in the Hardware Status register. The TX Ready bit in the Transmit Data Buffer drives the TX Ready bit and also TXDREQ via the DMA logic.

After reset, this bit is zero.

Frame Size   The Frame Size field determines the number of words contained in the data buffer. It acts as the reference input to the host buffer address comparator.

ADDRESS COUNTER

The 5-bit address counter provides the sequential buffer access address for access by the host via the Host Data Buffer access port. The address counter is reset to zero when the CT8020 writes a 1 to the TX Ready bit of the internal control register causing control of the buffer to transfer to the Host. Each time the host accesses the upper byte of the Host Data Buffer access port the address counter increments by 1.

The data buffer access port is only physically 8-bits wide. When an access to this port is made by a host processor, the byte select address line HSTAB0 is valid and can be used to select the byte accessed. When access is made by a DMA controller, the address decode which selects the data buffer access port is provided by the TXDACKN signal. During a DMA cycle, the HSTAB3-0 address bits are not valid. Generation of an internal HSTAB0 is thus required to select the byte accessed. This is provided by a simple toggle mechanism which changes state on each DMA access. The DMA byte select toggle is set to zero each time the TX Ready bit changes from a zero to a one (this also clears the main address counter). A separate DMA byte select toggle is required for transmit and receive.

COMPARATOR

The 5-bit comparator is active only when the Host has control (the TX Ready bit is set). The comparator compares the value in the address counter with the value in the Frame Size field. If the values are not equal, the host continues to have access to the data buffer. When the values become equal (after the last host access), the TX Ready bit is reset, transferring control back to the CT8020.

TRANSFERRING DATA FROM HOST TO CT8020

The CT8020 determines the size of the data frame to be transferred by some protocol with the Host. At the beginning of data transfer, the TX Ready bit will be zero. The CT8020 then programs the Frame Size and sets the TX Ready bit (in the same write cycle). This causes the TX Ready bit visible in the Hardware Status Register to be set. The host discovers that the TX Ready bit is set (by polling or interrupt). The Host then writes Frame Size words into the Host Transmit Buffer Access Port, after each word is written, the address counter increments. When the Host writes the last word, the address counter is incremented and matches the Frame Size value. This is detected by the comparator which causes the TX Ready bit to be cleared. The CT8020 discovers that it has access to the data buffer and reads the buffer contents, transferring them to the CT8020's local RAM. This process is repeated to transfer the next frame.

For DMA transfers, the TX Ready bit drives the state of the DMA Request signal. When TX Ready is set, the DMA request is asserted. When the buffer becomes full, and buffer control automatically returns to the CT8020, the TX Ready bit is cleared and the DMA Request signal is de-asserted.

4.6 DMA Transfers

The CT8020 is intended to interface directly to one or two external 8-bit DMA controllers connected to the host bus. The DMA controllers may be of the "fly-by" type (used in IBM compatible PCs) or the "flow-through" type (for example -used in the Intel 80186).

In a fly-by DMA transfer, the DMA controller simultaneously generates the address of the source or destination memory location, the read/write signal to the memory, a read/write signal to the peripheral, and a DMA acknowledge signal (which enables the destination or source peripheral). In a "read from peripheral" cycle, the DMA Acknowledge signal plus the peripheral read strobe, cause the peripheral to gate its' data onto the data bus. The DMA controller provides the destination memory address and asserts the memory write signal causing the peripheral's data to be written to the memory. In a "write to peripheral cycle", the DMA controller generates the memory address and asserts the memory read signal causing the appropriate data byte to appear on the data bus. The DMA controller also asserts the DMA Acknowledge signal plus the peripheral write strobe, which causes the peripheral to read the data currently on the data bus. This type of DMA controller requires DMA request **and** DMA acknowledge signals. The address signals are ignored by the peripheral, since they indicate the memory address not the peripheral address. Instead the peripheral uses the DMA acknowledge signal plus the read/write strobe to indicate that it has been selected.

The alternative type of DMA controller which uses a "flow-through" transfer is supported by the normal host processor data transfer interface. In a flow-through transfer, the read/write access to the peripheral and the write/read memory access are performed as two separate cycles, with the DMA controller providing temporary storage of the data. In this type of transfer, the DMA access cycle to the CT8020 is identical to a host processor access cycle. In a "read from peripheral" cycle, the DMA controller first drives the address bus with the address of the peripheral, and asserts HSTCS/ and HSTRD/. The DMA controller temporarily saves the peripheral data and then writes the data to memory by performing a normal memory access cycle. This type of controller requires the DMA request signals **only**, and does not use the DMA acknowledge. When used with this type of controller, the CT8020 DMA acknowledge signals should be connected to VCC via pull-up resistors.

4.6.1 DMA modes

The DMA interface can be operated in two modes : full-duplex and half-duplex.

4.6.1.1 Full-Duplex Mode

In Full-Duplex mode, the RX and TX DMA interfaces operate independently of each other, with physically separate control signals dedicated to the two data transfer directions. Two external DMA channels are required.

4.6.1.2 Half-Duplex Mode

In Half-Duplex mode, only a single external DMA channel is required. The external DMA controller will have only a single DMA Request line available and a single DMA Acknowledge line. Using only these two signals, the DMA controller must be able to transfer data both to and from the CT8020. To accommodate this arrangement without requiring external glue logic, the TXDREQ and RXDREQ and the TXDACKN and RXDACKN pin functions can be swapped by the host using the control bits in the Hardware Control Register. This allows the DMA controller to be hard-wired to one set of DMA pins, and permits software control of the transfer direction associated with those pins.

4.6.2 Burst Mode and Single Cycle Mode Transfers

DMA transfers can be performed in either Burst Mode (continuous) or Single Cycle mode. In Burst Mode, the DMA request signal TXDREQ or RXDREQ remains asserted whenever the appropriate data buffer can accommodate the transfer. Each time the DMA acknowledge signal, TXDACKN + HSTWRN or RXDACKN + HSTRDN, is asserted a byte is transferred. This continues until the Transmit Data Buffer is full or the Receive Data Buffer is empty, at which point the DMA request signal is de-asserted (the appropriate TX or RX Ready bit is cleared). Burst Mode allows for the fastest transfer of data, since the Host is required to perform bus request/bus grant arbitration with it's external DMA controller only once per burst. With a 16-word buffer, up to 32 bytes can be transferred in a single burst.

In Single Cycle mode, the DMA request signal, TXDREQ or RXDREQ is asserted then de-asserted once for each byte transferred. This mode requires the Host to re-arbitrate bus access with the external DMA controller for each byte transferred. When the CT8020 is ready to perform a DMA transfer, the DMA request signal is asserted. The DMA controller responds with the DMA acknowledge signal (plus HSTRD/ or HSTWR/) which clocks the byte data transfer and also causes the DMA request signal to be withdrawn. After the byte transfer has completed, the CT8020 delays for a short period of time and then re-asserts the DMA request signal (assuming it has more data to transfer).

Single Cycle Mode
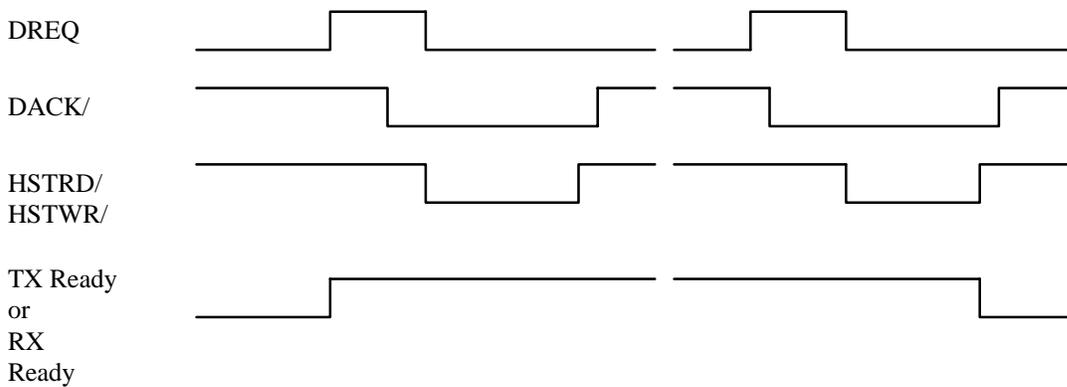
Figure 4-4 Single Cycle DMA mode

In single cycle mode, the negative going edge of HSTRD/ or HSTWR/ during DACK/, causes the DREQ signal to be de-asserted. If RX or TX Ready bit is still set after the end of the DMA cycle, then DREQ will be re-asserted 16 MAINCLOCK clock periods after the positive going HSTRD/ or HSTWR/ edge. At 40 Mips (25ns) this translates to 400 ns. The address counter used to index the data buffer during Host/DMA cycles is incremented by the positive going edge of HSTRD/ or HSTWR/ on alternate DMA cycles (i.e. each time a high byte is accessed). The data buffer block contains a toggle bit which is used to generate a DMA byte select. This toggle bit is used in place of HSTAB0 during a DMA cycle, it changes state at the end of each DMA cycle to provide the correct byte access sequence : low-byte, high-byte, low-byte, high-byte etc. The host address lines HSTAB3-0 are ignored during a DMA cycle. The toggle bit is set to zero, each time the data buffer address counter is reset (when the CT8020 writes a 1 to the RX or TX Ready bit). If the counter reaches the Frame Size limit value, then the RX or TX Ready bit is reset following the positive HSTRD/ or HSTWR/ edge.

Burst Mode

DREQ

DACK/

HSTRD/
HSTWR/
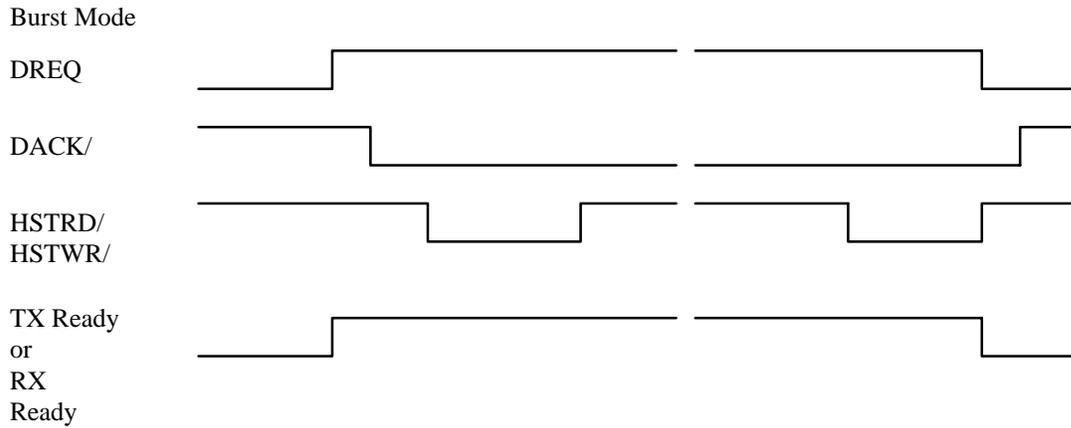
TX Ready
or
RX
Ready

Figure 4-5 Burst Mode DMA

In Burst mode, DREQ remains asserted until the RX or TX Ready bit is cleared by the final counter increment. Byte transfers are clocked by the HSTRD/ or HSTWR/ signals as appropriate. The positive going edge of these signals toggle the DMA byte select. The data buffer address counter increments on alternate cycles, i.e. each time a high byte is accessed. When the counter reaches the Frame Size limit the RX or TX Ready and DREQ signals are cleared.

4.6.3 Flow-Through DMA Transfers

PROGRAMMERS NOTE:

A "Flow-Through" DMA transfer is one in which the read and write operations of the DMA transfer take place as separate cycles, with the DMA controller providing intermediate temporary storage of the data. In this type of DMA, the data physically "flows through" the DMA controller:

DMA controller outputs source address
DMA controller reads from source
DMA controller stores data in internal temporary register (single byte)
DMA controller outputs destination address
DMA controller writes data to destination.

Figure 4-6 Flow-Through DMA
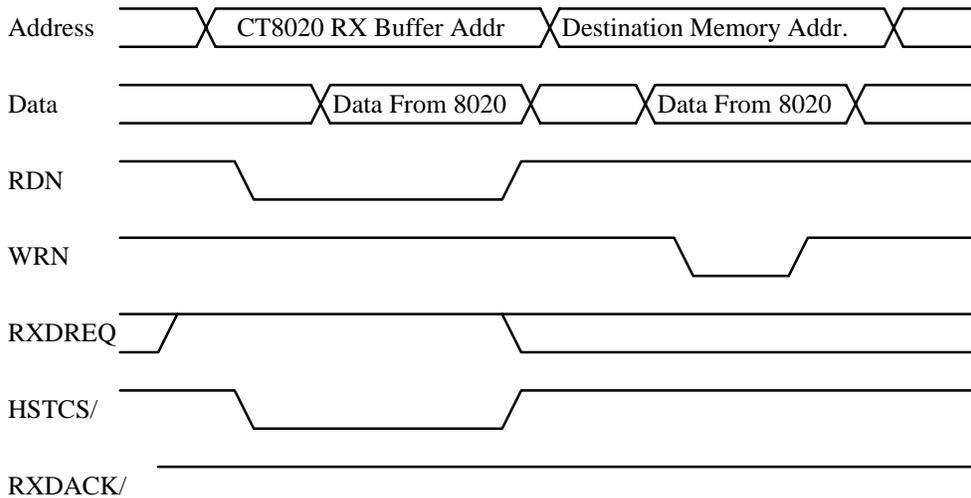
Example of a CT8020 to Memory DMA transfer using "Flow-Through" DMA. The RXDACK/ signal is not used.

Note that, from the perspective of the CT8020, an access by a "Flow-Through" type DMA controller looks identical to a normal Host access. The Intel 80186 and 80188 processors contain this type of DMA controller.

5. CT8020 CODEC INTERFACE
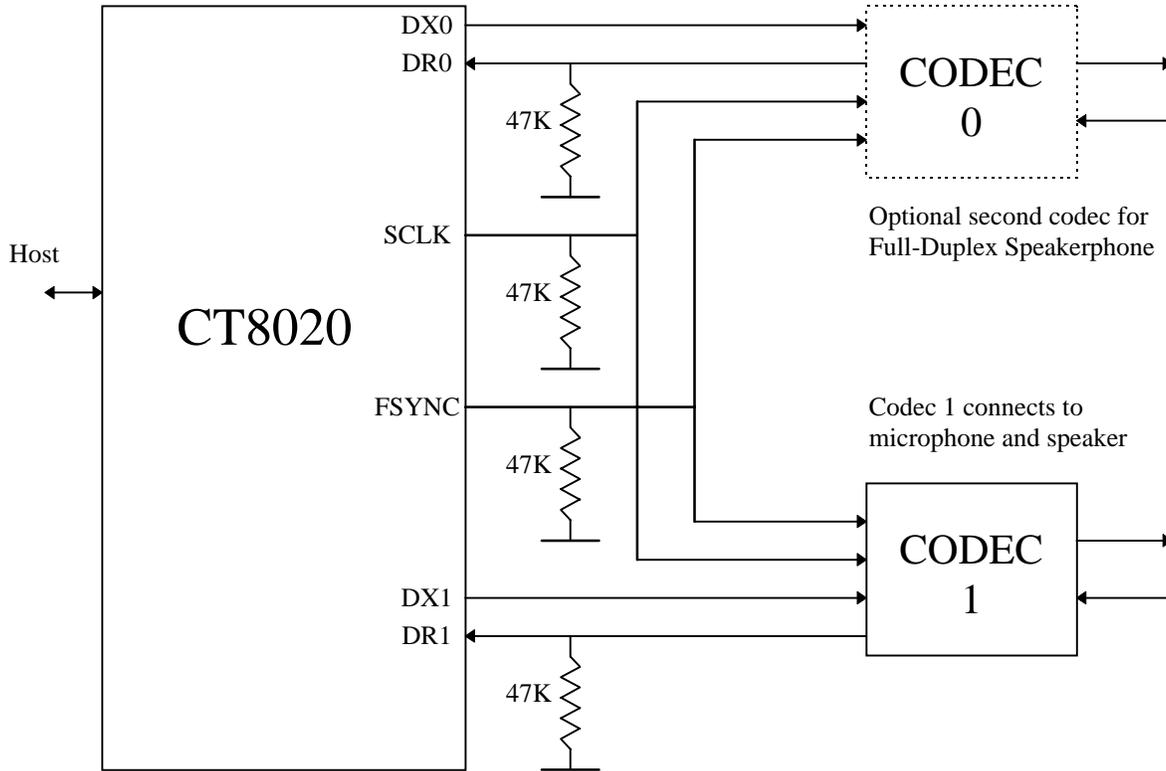
Figure 5-1 CT8020 Codec Interface connection

In Master mode, the CT8020 generates the FSYNC and SCLK signals.

In Slave mode, the FSYNC and SCLK signals are generated externally. In slave mode, the CT8020 FSYNC and SCLK pins are inputs.

Note that during and after reset, the SCLK and FSYNC pins are configured as inputs. As such, they require external pull-down resistors to ensure that a safe and defined logic level is present.

5.1 Codec Options

The CT8020 codec interface supports the following features:

- Codec clock master or slave
- 8-bit A-law/Mu-law or 16-bit linear codec
- Short or Long FSYNC
- programmable SCLK and FSYNC clock rates

5.1.1 Master/Slave

The CT8020 can be operated in codec master or slave mode.

In master mode, the SCLK and FSYNC signal pins are outputs. The clock frequencies for the two signals are generated by integer division from the internal CT8020 DSP core clock. To achieve a SCLK frequency of 2.048 MHz for operation with a A-law or Mu-law codec, the CT8020 internal clock should be 38.912 MHz (3.8912 MHz crystal). If operating from an external 4.0 MHz crystal, SCLK may be selected as 2.0 MHz and FSYNC 8.0 KHz. Normally, a standard telecom A-law or Mu-law codec will operate correctly with SCLK at 2.000 MHz with the exception that the bandwidth of the codec anti-aliasing filter will be slightly reduced.

In slave mode, the SCLK and FSYNC signals pins are inputs. The SCLK and FSYNC signals must be generated externally. For TrueSpeech operation the FSYNC frequency should be exactly 8.0 KHz. In this mode, the CT8020 internal clock may be 40 MHz (4 MHz crystal). In slave mode it is possible to connect the CT8020 codec interface to a TDM (Time Division Multiplexed) bus.

Following reset, the CT8020 codec interface will be in slave mode, so that SCLK and FSYNC are inputs.

5.1.2 8-bit A-law/Mu-law and 16-bit linear codec

The CT8020 codec interface can be programmed by the host to operate in 8-bit or 16-bit mode. In 8-bit mode for each FSYNC, 8 data bits are shifted out of the DX0 and DX1 pins, and 8 data bits are shifted in at the DR0 and DR1 pins. In 16-bit mode for each FSYNC , 16 data bits are shifted out of the DX0 and DX1 pins, and 16 data bits are shifted in at the DR0 and DR1 pins.

In 8-bit mode, the data format may be either Mu-law or A-law.

In 16-bit mode, the data format is 16-bit linear, with the m.s. bit shift in/out first.

5.1.3 Short or Long FSYNC

In master mode, the CT8020 may be operated in short or long FSYNC mode. In short FSYNC mode, the FSYNC pulse is 1 SCLK period wide. The timing of the FSYNC pulse relative to the data bits conforms to the telecom industry standard for short FSYNC for PCM A-law/Mu-law codes when SCLK = 2.048 MHz and FSYNC = 8.00 KHz. In long FSYNC mode, the FSYNC pulse is 8 or 16 SCLK periods wide depending on the data width selected. In this mode, the FSYNC pulse is aligned with the receive and transmit "time slot" of the data bits.

In slave mode, the width of the FSYNC pulse is not important. Selecting long or short FSYNC mode, only affects the assumed timing position of the FSYNC relative to the data bits.

5.1.4 Programmable SCLK and FSYNC rates

In master mode, the SCLK and FSYNC rates are programmable by the host.

SCLK is generated by a division-by-(N+1) from the internal CT8020 clock. The divisor may be in the range $4 <= (N+1) <= 32$. If the internal CT8020 clock is 38.912, then setting N = 18 will produce a 2.048 MHz SCLK.

FSYNC is generated by a division-by-(M+1) from SCLK. The divisor may be in the range $18 <= M <= 1023$. If SCLK = 2.048 MHz and M = 255, then FSYNC will be 8.0 KHz.

The table below shows possible clock frequencies

MAINCLOCK = 38.912 MHz (3.8912 MHz crystal)			
SCLK	FSYNC	N	M
2.048 MHz	8.000 KHz	18	255
2.048 MHz	11.011 KHz	18	185

PCM Mu-law / A-law CODEC filter bandwidth = 3.40 KHz (nominal)

MAINCLOCK = 40.000 MHz (4.000 MHz crystal)			
SCLK	FSYNC	N	M
2.000 MHz	8.000 KHz	19	249
2.000 MHz	11.050 KHz	19	180

PCM Mu-law / A-law CODEC filter bandwidth = 3.32 KHz (nominal)

Note that the AT&T T7525 16-bit linear codec requires that the SCLK frequency is exactly 256 times the FSYNC frequency. When using this codec SCLK must be 2.048 MHz in order to achieve a FSYNC frequency of 8.000 KHz.

For an 8-bit codec, the CT8020 requires that the SCLK frequency is at least 16 times the FSYNC frequency.
For a 16-bit codec, the CT8020 requires that the SCLK frequency is at least 32 times the FSYNC frequency.

5.1.5 Stop Codec

In Master mode, the STOP CODEC command can be used to halt operation of the codec interface. In this state the FSYNC and SCLK signals are held low. Stop Codec in Slave mode has no effect.

6. HOST DATA TRAN SFER MODES

Data transfer between the CT8020 and host can be performed in two ways:

- via the Transmit and Receive Data Buffers (recommended for new designs)
- via the Software Control and Software Status Registers (CT8015 compatible mode)

6.1 Data Transfer using the Data Buffers

This transfer mode is recommend for all new designs.

In this mode, the CT8020 supports DMA transfers as well as low-overhead host processor based transfers. Once the CT8020 playback/record options have be selected and activated, speech frames can be transferred with minimal or zero "control overhead" required for device polling or supervision.

6.1.1 DMA Transfers

The CT8020 provides a full-duplex DMA interface with independent Transmit and Receive, request and acknowledge signals. The host issues the commands to the CT8020 to start playback and/or record, then enables DMA transfers by programming the Hardware Control Register. Once playback/record operation has been setup, the CT8020 can continue to transfer speech frames without further involvement of the host. The host processor can optionally use the buffer management commands to observe and control the status of the speech data streams.

6.1.2 Host Processor Transfers

In systems where no DMA controller is available, the host processor can be used to perform the data transfers. The playback and/or record operation is setup as before, then the host processor can either configure the Hardware Control Register to generate an interrupt to the host on the TX/RX ready condition, or alternatively, the host may simply poll the TX/RX ready status periodically. Once the host is ready to perform the data transfer, it can perform read/write "bursts" of up to 16 words of data without needing to re-check the TX/RX ready status. The data buffers can contain a maximum of 16 words of data. This size is sufficient to accommodate a complete TrueSpeech data frame. This allows microprocessors with "repeat" instruction prefixes (e.g. Intel X86 : REP INS, REP OUTS) to perform block moves of compressed speech frames. When performing record/playback of non-compressed data, where the speech data frame size is greater than 16 words, the host may divide the data transfer into 16-word sub-blocks and re-check the TX/RX ready status between the sub-blocks.

6.2 Data Transfer using the Software Control and Status Registers

This transfer mode is provided for software compatibility with the CT8015 and CT8005.

In this mode, the CT8020 supports data transfers using only the Software Control and Status Registers. This mode provides backwards compatibility with the data transfer protocol used in the CT8005 TrueSpeech 8.5 Messaging Co-Processor and the CT8015 TrueSpeech 8.5 DSVD Co-Processor. To perform data transfers,

the host must interrogate the CT8020 using the playback/record "C2-S2-C3-S3" command/status sequence. When the CT8020 is ready to transfer data, it returns the available transfer count in the "S3" status response. The host then performs the required number of command-write-status-read cycles using the Software Control and Status registers to transfer the data.

6.2.1 Host Control/Status Register Data Transfer Synchronization Modes

The synchronization modes described here, are intended for use with speech data transfers **performed via the Software Control and Status Registers only**. The synchronization options control the manner in which data transfers are coordinated with control operations performed via these registers. When data is transferred via the transmit and receive data buffers, the CT8020 provides dedicated TX/RX ready/DMA signals.

The rate of transfer of data between the host and the CT8020 must, in general, be synchronized with the rate at which speech data is transferred between the CT8020 and its external codec(s). Data is exchanged between the CT8020 and the codec, one sample every 125 micro-seconds (at 8.0 KHz). This data is accumulated into blocks of 240 samples which corresponds to a period of 30 milliseconds. If the channel is operating in a-law/mu-law or linear mode etc., this data block (or frame) is transferred to the host without compression. If the channel is operating in TrueSpeech mode (compressed), the frame is compressed before transfer. The 30 ms period is derived from the external codec clock by counting 240 samples.

The CT8020 devices are intended to be used in pairs, at opposite ends of a communications link. The CT8020 at each end of the link, will have its own external codec and its own independent clock source or crystal. Data is moved between the two devices in real-time via the host processors attached to each CT8020 at each end of the link. Even though the CT8020 clocks will probably be derived from a crystal source, to generate the 8.0 KHz codec sample rate, the precise frequencies of these clocks will most likely be fractionally different. The frequencies may well also vary with temperature and time. As a result of this, one CT8020 at one end of the link will source/consume speech data at a fractionally different rate from the CT8020 at the other end of the link. Over time this difference will accumulate, if left alone. If the playback channel at one end, consumes data more slowly than it arrives, the transmit buffer queue will gradually fill, increasing the apparent transmission delay until the transmit buffer queue becomes full. At this point frames of data will begin to be discarded. If the playback channel consumes data more quickly than it arrives, the transmit buffer will become empty over time until the playback channel becomes starved of data. At this point gaps will be introduced into the outgoing speech, or extra frames of data will have to be synthesized to make up for the short fall in frames.

To assist with dealing with this end-to-end synchronization problem, the CT8020 playback and receive channels can be operated in one of four different sync modes. The sync mode of operation of the playback (transmit) and record (receive) channel can be selected independently. The Codec Sync mode provides for backward software compatibility with the CT8005 TrueSpeech Messaging Co-Processor.

The four sync modes are:

1. Codec Sync Mode
2. Data Sync Mode
3. Poll Sync Mode
4. Host Sync Mode

6.2.1.1 Codec Sync Mode

In Codec sync mode, Host-Codec synchronization is maintained on a 30 ms frame-by-frame basis. The CT8020 does not perform any additional internal buffering. This mode provides minimum delay with the tightest coupling between codec-CT8020 transfers and CT8020-host transfers (there is a 1 frame delay). In this mode, the Host must ensure that it is able to perform a data transfer every 30 ms. Data transfers are performed by the host processor and take place through the Software Control and Status Registers. This mode is compatible with the data transfer protocol used by the CT8005 TrueSpeech Messaging Co-Processor. In this protocol the playback/record command sequence is directly synchronized with the 30ms frame rate by delaying the Status responses until the frame is ready. This causes the CT8020 host interface to "block" or "wait" on a command to transfer data. This blocking means that this mode can only support half-duplex data transfers, i.e. concurrent playback/record is **not** supported in this mode. While the command/status interface is blocked waiting for the next frame, the CT8020 is unable to process other commands. The blocking effect also means that only 1 frame can be transferred to the CT8020 each frame period. As a result of this the effective buffer depth of the CT8020 is 1, regardless of the buffer limit setting. Software designed to support the CT8005 may depend on the blocking feature in order to use the rate at which the CT8005 responds in order to measure the progress of time. Also, this mode has the property that a data frame can always be transferred once the CT8020 has returned a status response (the transfer count returned in the S3 status response is always non-zero). Codec Sync Mode is the default mode of the CT8020 following reset.

6.2.1.2 Data Sync Mode

This mode is intended to operate in a similar manner to the Codec Sync mode, with the difference that additional buffering is provided within the CT8020. This relaxes the requirement that the host be able to respond to a transfer request from the CT8020 every 30 ms (depending on the buffer limit set). This mode provides a degree of compatibility with the CT8005 TrueSpeech Messaging Co-Processor, while also providing additional buffering.

Blocking of the command/status interface can be avoided, in this mode, by using the buffer depth polling commands prior to issuing the data transfer (play/record) commands. By checking the buffer depth, the host can avoid reading from an empty record buffer, or writing to a full playback buffer.

This mode is automatically selected when the CT8020 enters host-to-host (codec-less) compression or decompression mode. This default can be over-riden by changing the sync mode after the start of host-to-host mode.

6.2.1.3 Poll Sync Mode

In Poll Sync mode, the CT8020 maintains internal frame buffers which are tied directly to the host interface transmit/receive data buffers. Available receive data is transferred automatically to the host interface receive buffer unless the buffer is full. Any data placed in the host interface transmit buffer is automatically transferred to the internal transmit buffer unless that buffer is full. This mode is recommended for DMA transfers where there is no frame-by-frame host supervision (no "C2-S2-C3-S3" play/record command sequence is required).

Poll Sync Mode is non-blocking variant of Data Sync Mode. Regardless of the data transfer option selected, the command/status responses occur without waiting to synchronize with the 30 ms frame period. When the record buffer is empty or the playback buffer is full, the CT8020 returns zero as the transfer count in the playback/record "S3" status response. Data may be transferred via the Software Control and Status Registers, via the transmit and receive data buffers using the host processor, or via the transmit and receive data buffers using a DMA controller.

6.2.1.4 Host Sync Mode

Host Sync mode is similar to Poll Sync mode, except that the host is always given permission to perform the transfer it requests, irrespective of the internal transmit and receive state. The CT8020 accommodates this by creating or discarding data as necessary.

6.3 Data Transfer Options Summary

The following table summarizes the data transfer options:

Sync Mode	Data Transfer Options		
	Host via Software Control & Status Registers	Host via Data Buffer	DMA via Data Buffer
Codec	X		
Data	X		
Poll	X	X	X
Host	X		

Poll Sync mode should be selected when performing data transfers via the transmit and receive data buffers. In this mode, data transfer can be performed by the Host processor itself, or using an external DMA controller.

7. PLAY & RECORD DELAY MANAGEMENT

7.1 Delay and Latency Management

The CT8020 provides features that allow the host to manage and control the amount of delay and latency provided by the CT8020. The CT8020 includes data buffering in both the playback and record channels which allows the host to operate with relaxed timing requirements when transferring data to or from the device. Internally, the CT8020 operates within a strict single frame 30 ms time limit when compressing and decompressing speech frames in real-time. The CT8020's buffering capabilities allow the host to operate with programmable additional latency so as to avoid requiring the host to perform data transfers that are synchronized exactly to the 30 ms frame period. By programming the buffer depth for the record and playback channels, the host can select the trade-off made between the time allowed for the host to respond to a request for data transfer and the amount of delay introduced. Also the host is able to manage any accumulation of data, which causes additional delay, that results from differences in precise clock rate between the two ends of a speech link.

7.2 Data under-run and over-run

Data over-run occurs when data arrives at a point faster than data departs from that point. Data under-run occurs when data attempts to leave a point faster than it arrives. In addition to providing buffer depth management support functions such as buffer depth monitoring and variable buffer depth control for host based buffer management, the CT8020 has a built-in or default buffer management scheme. When the host allows the record (receive) buffer to over-run, the CT8020 responds by simply discarding frames until the host causes the record buffer to become non-full. When the host allows the playback (transmit) queue to become empty, the CT8020 responds by repeating the last frame until new data becomes available.

7.3 Buffer Monitoring

The CT8020 provides buffer monitoring functions which allow the host to determine at any point in time, the amount of speech data in the device's transmit and receive queues.

7.4 Frame creation and deletion

The CT8020 provides frame creation and deletion commands to allow the host to control dynamically the transmit and receive speech channel delays. The frame creation function causes the CT8020 to create an extra frame (provided the relevant queue is not full) by duplicating the most recent frame. The frame deletion function causes the CT8020 to discard the most recent frame from its receive or transmit buffers (assuming the buffers are not empty). These functions are an essential part of managing a full duplex communications link for two reasons.

The first is that, since the clock rates at the two ends of the link will always be fractionally different, one end of the link will tend to accumulate data, progressively increasing the end-to-end delay. The other end will consume data more quickly than it arrives. This causes any intentional delay or speech buffer created by the host, for the purpose of "smoothing" or averaging out of the data transmission rate, to be gradually consumed, until the link operates with zero delay. The creation and deletion functions allow the host to monitor the buffer depths continually and introduce periodic corrections to the overall effective data rate to keep the buffers filled to the desired depth. For example, if the host detects that the transmit buffer depth has become too low, it can correct this by instructing the CT8020 to create an additional frame.

The second reason is that, since the communications link connecting the two ends of the speech channel may be prone to occasional errors or data corruption, then speech frames will, from time-to-time get lost or damaged and thus discarded. This has the same effect as the data under-run process. Again, the host can use the frame create function to make up for the lost frames. If the host-to-host link includes error correction, this second issue will not be a problem. However, use of error correction schemes either entails a higher bit rate (in the case of forward-error correction) or increased latency (delay) in the case of error correction by error-detection-and-re-transmission. Both the techniques are usually undesirable on real-time speech links. The host-to-host link should include some kind of error detection mechanism (e.g. checksum or CRC) so that the host can detect corruption of speech data frames. Since the speech is very highly compressed using TrueSpeech, every bit in the speech frame is significant. If a single bit is in error, a major disturbance (noise) may be generated in the speech signal if the damaged frame is decoded. In this situation, the host should detect and discard damaged speech frames and instruct the CT8020 to create a (undamaged) frame to replace it. This process of detection, discarding and replacement of damaged frames is also known as "frame erasure".

Note that the G.723.1 includes a built-in frame erasure mechanism for performing replacement of missing or corrupt speech frames. The G.723.1 frame erasure system (for use with the 6.3, 5.3, 4.8 and 4.1 rates) is independent of the mechanism described above. The G.723.1 frame erasure system performs an intelligent extrapolation of data from previous speech frames in order to replace missing frames. This feature is activated by use of specially coded speech frames.

7.5 Buffer Freezing (Pausing)

The CT8020 supports freezing or pausing of the transmit and receive buffers. Freezing of the transmit (playback) queue enables the host to pre-load frames into the playback channel before the start of playback. In a system where the host deliberately introduces delay into the channel for the purpose of smoothing an un-even data transmission rate, this feature allows the host to make use of the CT8020 internal buffer space to store the "speech reservoir" used for smoothing.

7.6 Variable Buffer Depth

The CT8020 includes 480 bytes each of buffer space for the playback (transmit) and record (receive) queues. In A-law/Mu-law or 8-bit mode, this is sufficient for two 240-byte mu-law frames (60 ms delay) or 15 32-byte TrueSpeech 8.5 frames (450 ms delay). In 16-bit mode, this space can hold only a single 480-byte frame (30ms). By default, the CT8020 will use all of this space. However, the host may wish to limit the amount of buffering the CT8020 uses in order to limit the maximum amount of delay in the speech channel. The CT8020 includes functions to set a limit on the effective buffer depths which is lower than the physical size for just this purpose.

7.7 Silence Generation During Transmit (Playback) Data Under-run

If data under-run occurs during playback, the transmit buffer becomes empty and the CT8020 will default to repeatedly outputting the most recent speech frame up to a (default) limit of 8 times. This behavior is appropriate to "mask" a short 1 or 2 frame period in which playback data is not available. Repeating the most recent frame 1 or 2 times causes the least perceptible break in the continuity of playback. However, if the data under-run condition persists for a longer period of time, the repeated playback of a single frame can cause annoyance to the user. The auto-repeat limit can be programmed by the host in the range 1-15.

Programming the auto-repeat limit to zero, will cause auto-repeat to operate continuously. When the auto-repeat limit is exceeded the CT8020 will output silence until more playback data becomes available.

7.8 Inserting Silence Frames during TrueSpeech Playback

The CT8020 will interpret TrueSpeech data frames that have all words set to zero as silence frames. Each time the CT8020 receives an all zero TrueSpeech frame it will output 30 ms of silence. This applies to all 5 TrueSpeech Rates 8.5, 6.3, 5.3, 4.8 and 4.1. Note that this is a CT8020 specific feature. It is not a part of the standard TrueSpeech or G.723.1 implementation.

8. Test Modes

The CT8020 supports special modes of operation to facilitate both in-system testing of the device itself and also as an aid to external system testing.

8.1 Test Mode 1: count mode

In this test mode, data received from the external A-law /Mu-law codec by the record channel is discarded and replaced by an incrementing count. This test mode is intended for use in A-law / Mu-law speech mode where the codec receive data is passed directly to the host (without compression, and with record volume set to nominal).

8.2 Test Mode 2: digital milliwatt

In this test mode, data received from the external mu-law codec by the record channel is discarded and replaced by the CCITT G.711 A-law / Mu-law digital milliwatt (0 dBm0) code sequence. This is a sequence of 8 repeating bytes (A-law Mu-law samples) representing a 1 KHz sinewave at 0 dBm0. Selection between A-law and Mu-law is made using the codec configuration command. Digital milliwatt operation is not supported for use with a 16-bit linear codec.

8.3 Test Mode 3: internal loopback

In this test mode, data received from the external A-law / Mu-law codec by the record channel is discarded and replaced by the output data from the transmit (playback) channel. The playback channel is not affected by this mode of operation. The playback speech data is transmitted to the output codec.

Note that receive codec to transmit codec loopback can be performed by the host with the CT8020 operating in normal mode. To do this, the host simply copies frames from the record (receive) channel back to the playback (transmit) channel using A-law, Mu-law, or 16-bit linear modes as appropriate .

8.4 Codec Loopback and Monitoring

The CT8020 also supports codec loop-back and monitoring configurations.

9. CT8020 HOST CONTROL PROTOCOL

9.1 Operational Modes

The CT8020 can be operated in 8 main modes:

1. Idle Mode. In this mode, the CT8020 transmit and receive buffers are empty. Data from the receive codec is ignored, silence is output to the transmit codec.
2. Playback mode. In this mode the playback buffer is active and the TrueSpeech frame decompression function operates (if in TrueSpeech mode). The host should provide data for output in this mode. If no data is available, the most recent frame present in the playback buffer is replicated and output until new data is available.
3. Record mode. In this mode, the record buffer is active and the TrueSpeech compression function operates (if in TrueSpeech mode), and proceeds to insert speech frames into the record buffer. The host should extract frames from the CT8020 in this mode. If the host does not take data from the CT8020, the record buffer will fill, and then frames will be discarded.
4. Full Duplex Speech mode. This mode is equivalent to the playback and record modes operating concurrently.
5. Codec Loopback Mode. This mode provides a test mode which enables codec-input to codec-output loopback.
6. Line Monitor Mode. In Line Monitor Mode the CT8020 provides DTMF and Call Progress Tone detection. These services are also available during record and playback operations.
7. Full Duplex Speech mode plus Acoustic Echo Canceller (AEC) (DSVD Speakerphone mode). In this mode the AEC is active and attempts to remove the acoustic echo of the speaker output that is picked up at the microphone input.
8. Full Duplex (Standalone) Speakerphone mode. In this mode the CT8020 operates as a Full Duplex Speakerphone using an analog telephone line connection. This requires operation with two external codecs. The codec0 connection must be used for the telephone line audio (analog) input/output. The codec1 connection must be used for the speaker-microphone audio input/output. In Full Duplex Speakerphone mode, the CT8020 attempts to cancel the speaker-to-microphone acoustic echo and also the telephone line transmit to telephone line receive electrical echo. See Appendix A.

Note: The terms "**Standalone Speakerphone**" and "**DSVD Speakerphone**" are used throughout this document to distinguish between Speakerphone operation in a conventional analog telephone environment and Speakerphone operation in a "hands-free" DSVD or Video Conferencing system (compressed digital speech via a modem or LAN).

9.2 Basic Protocol

The Host controls the CT8020 via a command-response protocol. For each command the Host writes to the CT8020, the CT8020 will generate a status response. The Host should read the response before issuing the next command.

Commands are written to the CT8020 via the Software Control Register. The CONTROL READY bit in the Hardware Status Register is set to indicate that the CT8020 is ready to accept a command. The Host should only write to the Software Control Register when the CONTROL READY bit is set. The CT8020 will respond to the command by writing a status response to the Software Status Register. The Host should wait for the STATUS READY bit in the Hardware Status Register to be set before reading from the Software Status Register. Reading from the Software Status Register will clear the STATUS READY bit.

Commands to the CT8020 are always result in an acknowledgment via the Software Status Register. The CT8020 registers are 16-bit. The Host accesses these registers using two 8-bit cycles: low byte then high byte.

Note: actual command value constants are presented in expanded 16-bit binary form and also where appropriate in hexadecimal form with the "X" value used to indicate user selected values. For example - the command 10XXH indicates that the "base" command is hexadecimal 1000H, but that the least significant 8 bits of the 16-bit command are user selected dependent on the command options desired.

9.3 Reset & Start-up Sequence

After RESET, the CT8020 performs internal initialization operations and then sets the CONTROL READY bit in the Hardware Status Register. The host should wait for this bit to be set before issuing the first command. After initialization the CT8020 enters idle mode and awaits a command from the host. The host should program the codec configuration before attempting further operations.

Operating Start-up Sequence:

1. Power-on or Reset.
2. Host polls Hardware Status Register and waits for CONTROL READY indication.
3. Host writes first command (IDLE = 0000H) to Software Control Register.
4. CT8020 generates command response (0000H) and sets STATUS READY.
5. Host waits for STATUS READY then reads response from Software Status Register.
6. Host writes CODEC configuration command to Software Control Register
7. CT8020 configures the codec (master/slave, A-law/Mu-law/16-bit and sample rate) and generates a status response.
8. Host waits for STATUS READY then reads response from Software Status Register.

Optional:

9. Host writes Get Device Identification Code = 3400H to the Software Control Register.
10. CT8020 responds with device code = 8020H and sets STATUS READY.
11. Host waits for STATUS READY then reads response from Software Status Register.

9.4 IDLE

Command :   0000H

Status: 0000H

The IDLE command instructs the CT8020 to enter IDLE mode. If the CT8020 is in either RECORD, PLAYBACK, FULL DUPLEX, or SPEAKERPHONE modes, speech processing is stopped. In IDLE mode, the CT8020 performs no processing except to wait for a command from the host.

IDLE should be the first command written to the CT8020 following reset.

9.5 CODEC CONFIGURATION

9.5.1 Codec Configuration Command

The CT8020 supports connection to two external A-law, Mu-law or 16-bit linear codecs labeled codec0 and codec1. Both codecs must be of the same type. Codec 1 is required for DSVD operation. Codec 0 is optional and is required only for standalone speakerphone mode. The data source for the record channel can be selected to be either codec, the data output for the playback channel can be selected to go to either codec or both codecs simultaneously.

After RESET, the Host MUST program the codec configuration before attempting any other operations (with the exception of Host-to-Host compression/decompression). Note that certain codecs may impose additional restrictions on the choice of the CT8020s external crystal or clock source frequency.

Command C1 (= C4XXH or C5XXH)

1100	010	Width	Law	Master	Long	OUTPUT CODEC	INPUT CODEC	Set Rate	0
(15-12)	(11-9)	(8)	(7)	(6)	(5)	(4-3)	(2)	(1)	0

Status S1

1100	010	Width	Law	Master	Long	OUTPUT CODEC	INPUT CODEC	Set Rate	0
(15-12)	(11-9)	(8)	(7)	(6)	(5)	(4-3)	(2)	(1)	0

Command C2 (only if Set Rate = 1, not required for slave mode operation)

WIDE	FSYNC_RATE	CO_RATE
(15)	(14-5)	(4-0)

Status S2 (only if Set Rate = 1)

WIDE	FSYNC_RATE	CO_RATE
(15)	(14-5)	(4-0)

Width   0 selects 8-bit A-law or Mu-law codec
                          1 selects 16-bit linear codec
                          (once WIDTH has been set, do not attempt to change this bit unless device has been
                          reset)

Law   0 selects external Mu-law codec
                          1 selects external A-law codec
                          (also affects Mu-law /A-law selection of RECMODE and PLAYMODE)

Master   0 selects slave mode (FSYNC and SCLK are inputs - default after reset)
                          1 selects master mode (FSYNC and SCLK are outputs)

Long   0 selects short frame sync mode when WIDE=0
                          1 selects long frame sync mode when WIDE=1

OUTPUT   00: default output codec routing
CODEC   01: output signal goes to codec 1 only
                          10: output signal goes to codec 0 only
                          11: output signal goes to both codec 0 and codec 1

INPUT   0 : normal input codec routing
CODEC   1: input from codec 0 and codec 1 are exchanged

Set Rate   0: no action
                          1: next command word programs codec sample rate dividers

CO_RATE   This field sets the division factor used to divide the main CT8020 clock to generate
                          SCLK. Division factor is (CO_RATE+1). For example 40 MHz / 20 = 2 MHz SCLK.
                          CO_RATE must be greater than 4.
                          (master mode only)

FSYNC_RATE   This field sets the division factor used to divide the SCLK clock to generate FSYNC.
                          Division factor is (FSYNC_RATE+1). For Example 2 MHz/250 = 8KHz.
                          F_SYNC_RATE must be greater than 17.
                          (master mode only)

WIDE   0: FSYNC is 1 SCLK period wide
                          1: FSYNC is 8 SCLK periods wide if Width=0 or 16 SCLK periods wide if Width=1.
                          Note that setting the WIDE bit to 1 only has an effect if the LONG bit is also set.

**Before entering Standalone Speakerphone mode, Output Codec must be set to 00 and Input Codec
set to 0.**

9.5.2 **Example codec configurations**

C1	C2	SCLK	FSYNC	Description
C442H	1F33H	2.000 MHz	8.000 KHz	Texas Instruments Mu-law TP3054 codec Short Frame Sync pulse Master Mode CO_RATE = 19 FSYNC_RATE = 249 external crystal = 4.000 MHz
C542H	1FF2H	2.048 MHz	8.000 KHz	AT&T 16-bit linear codec T7525 Short Frame Sync pulse Master Mode CO_RATE = 18 FSYNC_RATE = 255 external crystal = 3.8912 MHz
C462H	9FF2H	2.048 MHz	8.000 KHz	OKI Semiconductor Mu-law MSM7543 codec Long (+ wide) Frame Sync pulse Master Mode CO_RATE = 18 FSYNC_RATE = 255 external crystal = 3.8912 MHz

Note that the AT&T T7525 16-bit linear codec **requires** that the FSYNC frequency is exactly 1/256 of the FSYNC frequency. When using this codec, the FSYNC_RATE value **must** be set to 255. In order to accommodate this requirement, when operating in Master Mode, the CT8020 **must** be driven from an external 3.8912 MHz crystal or clock source .
For 8-bit codecs the SCLK frequency must be at least equal to FSYNC x 16.
For 16-bit codecs the SCLK frequency must be at least equal to FSYNC x 32.

Other codecs may permit a range of values for the FSYNC to SCLK ratio, however, note that for some codecs (e.g. TP3054 or TP3057) the actual usable range of ratios may depend on selection of the default or nominal ratio based on certain control pins. Depending on the operational mode selected, the TP3054 and TP3057 can support nominal ratios of 1:256, 1:193 and 1:192 using nominal 2.048 MHz, 1.544 MHz and 1.536 MHz values for SCLK. Informal tests have shown that the codecs can support ratio ranges of at least +/- 5% centered about these nominals.

9.6 RECORD

Command (C1 = 1XXXH):

0001	11	RECMODE	0	0	000	TFR Mode
(15-12)	(11-10)	(9-7)	(6)	(5)	(4-2)	(1-0)

Status (S1):

0001	11	RECMODE	0	0	000	TFR Mode
(15-12)	(11-10)	(9-7)	(6)	(5)	(4-2)	(1-0)

9.6.1 Transfer Mode

The TFR Mode field is used to select the mode of data transfer used:

TFR Mode	Data Transfer Mode
00	Data Transfer via Software Command and Status Registers (CT8015/CT8005 protocol mode). See section on Host Data Transfer Modes and Record Protocol.
01	Reserved
10	Reserved
11	Data Transfer via Host Transmit Data Buffer Access Port. Poll Sync Mode should be selected when using this data transfer option. This data transfer mode must be selected if performing DMA transfers using the TXDREQ and TXDACKN signals. See section on Host Data Transfer Modes and Record Protocol.

The following C2, C3 and Data Transfer commands are required only if TFR Mode = 00 (CT8015 / CT8005 protocol mode). See section on Record Protocol. These commands are used only if transferring speech data via the Software Control and Status Registers. For new designs using TFR Mode = [binary] 11 is recommended.

Command (C2 = 1000H):

0001	0000	0000	0000
(15-12)	(11-8)	(7-4)	(3-0)

Status (S2):

0001	F3	F2	F1	F0	0	PEAK	DTMF VALID	CPF VALID	DTMF DIGIT
(15-12)	(11)	(10)	(9)	(8)	(7)	(6)	(5)	(4)	(3-0)

Command (C3 =10XXH):

0001	0000	REQUEST NUMBER OF WORDS TO TRANSFER
(15-12)	(11-8)	(7-0)

Status (S3):

0001	0000	**ACTUAL** NUMBER OF WORDS TO TRANSFER
(15-12)	(11-8)	(7-0)

The NUMBER OF WORDS TO TRANSFER should either be set to the frame size of the selected speech mode, or set to zero to indicate no transfer is to take place.

Data Transfer Command:

0001	0000 0000 0000
(15-12)	(11-0)

Data Transfer Status:

16-bit speech data word
(15-0)

9.6.2 Recording Modes

RECMODE	Frame Size (words)	Recording Modes
000	16-8	TrueSpeech (8.5, 6.3, 5.3, 4.8 and 4.1) - See : Select TrueSpeech Record Rate command
001		Reserved
010		Reserved
011		Reserved
100	120	64 Kbit/sec A-law / Mu-law PCM (120 words per 30ms data frame)
101	240	128 Kbit/sec 16-bit linear (240 words per 30ms data frame)
110	120	64 Kbits/sec 8-bit signed linear (120 words per 30 ms data frame)
111	120	64 Kbits/sec WSS 8-bit unsigned linear (120 words per 30 ms data frame)

Notes:
1. All data rates assume that the codec connected to the CT8020 operates at 8000 samples/sec
2. The 30 ms frame interval is based on counting 240 samples from the codec.
3. Mode 100, PCM A-law / Mu-law is a "pass through mode", where the data from the codec is passed to the host entirely unmodified, (provided that the record volume is set to 0100H).
4. 16 bit linear data is signed integer (2's complement form), positive full scale is 7FFFH, negative full scale is 8000H, zero is 0000H
5. 8 bit linear data is signed byte (2's complement form), positive full scale is 7FH, negative full scale is 80H, zero is 00H
6. 8 bit linear WSS data is unsigned byte, positive full scale is FFH, negative full scale is 00H, zero is 80H. This is the format used for 8-bit WAVE format data (Windows Sound System). Data can be converted between the two 8-bit formats by simply inverting the ms bit.
7. The TrueSpeech rate 8.5,6.3,5.3,4.8 or 4.1 kbps is selected using the Select TrueSpeech Rate command

8. Selection between A-law / Mu-law is made using the codec configuration command. With an external Mu-law codec configured, RECMODE = 100 selects Mu-law data. With an external A-law codec configured, RECMODE = 100 selects A-law data.
9. The RECMODE and PLAYMODE bit assignments are different.

9.6.3 Peak Level Indication

The PEAK bit in the S2 status response is set if the average input level for the current speech frame exceeds the threshold configured using the Set Peak Threshold command. This bit can be used by the host to perform silence detection during recording. Note that the Record signal level can also be accessed using the Read Record Level command. This is the recommended method of determining the record input signal level, when TFR Mode = [binary] 11 and the C2-S2, C3-S3 sequence is not used.

CPF F3-0 and DTMF Detection: refer to section on Line Monitoring

9.6.4 Record Protocol

Example 1 : TrueSpeech 6.3 Record via Host Receive Data Buffer Access Port - Host Polling

This example shows how to start recording using TrueSpeech 6.3 with data transfers performed via the Host Receive Data Buffer Access Port. All data transfers in this example are performed by the host controller. The Host polls the Hardware Status Register to perform data synchronization.

Starting Record

1. CT8020 is in IDLE or PLAYBACK state.
2. Host checks for CONTROL READY state in Hardware Status Register.
3. Host selects TrueSpeech 6.3 recording by writing the Select TrueSpeech Record Rate command = 5131H to the Software Control Register.
4. CT8020 responds via the Software Status Register
5. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register. This clears the STATUS READY bit.
6. Host selects Poll Sync Mode for record using the command 5102H.
7. CT8020 responds via the Software Status Register.
8. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register. This clears the STATUS READY bit.
9. Host selects Record by issuing the RECORD "C1" command = 1C03H via the Software Control Register. This also informs the CT8020 that data transfers will occur via the Host Receive Data Buffer Access Port (TFR Mode = [binary] 11).
10. CT8020 performs internal synchronization then responds with the RECORD "S1" status response.
11. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register. This clears the STATUS READY bit.

The CT8020 is now in record mode. The CT8020 will produce a compressed speech frame every 30 ms. The following sequence is used to transfer each compressed speech data frame from the CT8020 to the host:

1. Host waits for the RX Ready bit to be set in the Hardware Status Register
2. Host reads 12 words (for TrueSpeech 6.3) from the Host Receive Data Buffer Access Port.

To terminate recording:

1. Host writes IDLE = 0000H command or STOP RECORD = 5120H command to the Software Control Register.
2. CT8020 terminates record and clears RX Ready if set (in Hardware Status Register).
3. CT8020 writes status response to Software Status Register.
4. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register. This clears the STATUS READY bit.

Note that after writing the IDLE or STOP RECORD command to terminate recording, the host should not attempt to access the Host Receive Data Buffer Access Port even if the RX Ready bit is set.

Example 2 : TrueSpeech 5.3 Record via Host Receive Data Buffer Access Port - Host Interrupt

This example shows how to start recording using TrueSpeech 5.3 with data transfers performed via the Host Receive Data Buffer Access Port. All data transfers in this example are performed by the host controller. The Host uses an interrupt service routine (ISR) to perform data transfer.

Starting Record

1. CT8020 is in IDLE state or PLAYBACK.
2. Host checks for CONTROL READY state in Hardware Status Register.
3. Host selects TrueSpeech 5.3 recording by writing the Select TrueSpeech Record Rate command = 5132H to the Software Control Register.
4. CT8020 responds via the Software Status Register
5. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register. This clears the STATUS READY bit.
6. Host selects Poll Sync Mode for record using the command 5102H.
7. CT8020 responds via the Software Status Register.
8. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register. This clears the STATUS READY bit.
9. Host selects Record by issuing the RECORD "C1" command = 1C03H via the Software Control Register. This also informs the CT8020 that data transfers will occur via the Host Receive Data Buffer Access Port (TFR Mode = [binary] 11).
10. CT8020 performs internal synchronization then responds with the RECORD "S1" status response.
11. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register. This clears the STATUS READY bit.
12. Host sets up an ISR to service interrupts from the CT8020.
13. Host programs the Hardware Control Register to generate an interrupt from the CT8020 on the RX Ready condition by writing 0401H (Master Enable set, RX Ready IE set).

The CT8020 is now in record mode. The CT8020 will produce a compressed speech frame every 30 ms. The following sequence is used by the Host ISR to transfer each compressed speech data frame from the CT8020 to the host:

1. Host gets interrupt from CT8020 (optionally checks that RX Ready is set).
2. Host reads 10 words (for TrueSpeech 5.3) from the Host Receive Data Buffer Access Port.

To terminate recording:

1. Host disables interrupts from the CT8020 by writing 0000H to the Hardware Control Register.
2. Host writes IDLE = 0000H command or STOP RECORD = 5120H command to the Software Control Register.
3. CT8020 terminates record and clears RX Ready if set (in Hardware Status Register).
4. CT8020 writes status response to Software Status Register.
5. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register. This clears the STATUS READY bit.

Note that after writing the IDLE or STOP RECORD command to terminate recording, the host should not attempt to access the Host Receive Data Buffer Access Port even if the RX Ready bit is set.

Example 3 : Linear 16-bit Record via Host Receive Data Buffer Access Port - Using DMA

This example shows how to start recording in uncompressed 16-bit Linear format speech with data transfers performed via the Host Receive Data Buffer Access Port. All data transfers in this example are performed by an external DMA controller.

Starting Record

1. CT8020 is in IDLE state or PLAYBACK state.
2. Host checks for CONTROL READY state in Hardware Status Register.
3. Host selects Poll Sync Mode for record using the command 5102H.
4. CT8020 responds via the Software Status Register.
5. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register. This clears the STATUS READY bit.
6. Host selects Record by issuing the RECORD "C1" command = 1E83H (RECMODE = [binary] 101) via the Software Control Register. This also informs the CT8020 that data transfers will occur via the Host Receive Data Buffer Access Port (TFR Mode = [binary] 11).
7. CT8020 performs internal synchronization then responds with the RECORD "S1" status response.
8. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register. This clears the STATUS READY bit.
9. Host programs external DMA controller to accept DMA requests from the CT8020 (See DMA Direction bit in Hardware Control Register). Host configures a data buffer in the Host memory to receive the DMA-ed speech data. The DMA memory buffer should be an integral multiple of the speech frame size. In the case of uncompressed 16-bit Linear, this should be N*480 (bytes).
10. Host sets up an ISR to handle an end-of-transfer (EOT) interrupt from the DMA controller when it reaches the end of the DMA buffer. Alternatively, if the DMA supports circular-buffering (auto-initialize), the Host can poll the DMA to determine when the end of the buffer is reached.
11. Host programs the Hardware Control Register to generate a DMA request from the CT8020 on the RX Ready condition by writing 0050H (RX DMA Burst Mode, RX DMA enable) - or 0150H (RX DMA Burst Mode, RX DMA enable, DMA Direction bit set).

The CT8020 is now in record mode. The CT8020 will produce a uncompressed speech frame every 30 ms. The following sequence occurs between the CT8020 and the DMA controller to transfer data:

1. CT8020 has 240 word (480 byte) uncompressed 16-bit speech data frame ready for transfer.
2. CT8020 transfers first 16 words into the Host Receive Data Buffer.
3. CT8020 asserts RX Ready.
4. RX Ready drives RXDREQ.
5. DMA controller responds to RXDREQ by asserting RXDACKN.
6. DMA controller performs a burst transfer of 16 words (32 bytes) from the CT8020 to the Host DMA memory buffer.
7. CT8020 de-asserts RX Ready.
8. CT8020 transfers next 16 words into the Host Receive Data Buffer.
9. CT8020 asserts RX Ready.
10. RX Ready drives RXDREQ.
11. DMA controller responds to RXDREQ by asserting RXDACKN.
12. DMA controller performs a burst transfer of 16 words (32 bytes) from the CT8020 to the Host DMA memory buffer.
13. CT8020 de-asserts RX Ready.
14. Repeat 8-13 until all 240 words of the speech data frame have been transferred.

The Host processor also needs to supervise the operation of the DMA controller and arrange for the transfer of the DMA-ed data to its final destination (e.g. transfer to disk). When the DMA controller reaches the end of the DMA buffer, the Host must process the data (transfer to disk). The Host can either arrange to receive

an EOT interrupt from the DMA controller, or can periodically poll the DMA's internal transfer count register to determine the status of the DMA.

To terminate recording:

1. Host disables DMA requests from the CT8020 by writing 0000H to the Hardware Control Register.
2. Host writes IDLE = 0000H command or STOP RECORD = 5120H command to the Software Control Register.
3. CT8020 terminates record and clears RX Ready if set (in Hardware Status Register).
4. CT8020 writes status response to Software Status Register.
5. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register. This clears the STATUS READY bit.

Note that after writing the IDLE or STOP RECORD command to terminate recording, the host/DMA should not attempt to access the Host Receive Data Buffer Access Port even if the RX Ready bit is set. When "cleaning up" at the end of recording, the Host should ensure that any partial frame at the end of the recording is discarded. When the recorded data is sent back to the CT8020 for playback, the CT8020 can only playback complete frames. It is recommended that the Host synchronizes the termination of recording with the end of transfer of a complete speech frame. This synchronization can be achieved by examining the DMAs transfer count register, or by performing the final speech data frame transfer using the Host processor.

Example 4: TrueSpeech 8.5 Recording using CT8005/CT8015 protocol via Software Control and Status Registers.

This example shows how to perform TrueSpeech 8.5 recording with TFR Mode = 00 using the CT8015 compatible protocol. Data is transferred via the Software Control and Status Registers. All data transfers are performed by the Host processor. The example shown uses the CT8015 Poll Sync Mode.

1. CT8020 is in IDLE or PLAYBACK state.
2. Host checks for CONTROL READY state in Hardware Status Register.
3. Host selects TrueSpeech 8.5 recording by writing the Select TrueSpeech Record Rate command = 5130H to the Software Control Register.
4. CT8020 responds via the Software Status Register
5. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register. This clears the STATUS READY bit.
6. Host selects Poll Sync Mode for record using the command 5102H.
7. CT8020 responds via the Software Status Register.
8. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register. This clears the STATUS READY bit.
9. Host writes Record C1 command = 1C00H (TrueSpeech 8.5) to the Software Control Register.
10. CT8020 activates record mode and performs internal synchronizations (1-2 frame delay) .
11. CT8020 responds with Record status S1 = 1C00H.
12. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register. This clears the STATUS READY bit.
13. **Host sends Record C2 command = 1000H.**
14. **CT8020 responds with Record S2 status = 10X0H, where X is defined by the PEAK bit state.**
15. **Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register. This clears the STATUS READY bit.**
16. **Host sends Record C3 with the number of (16 bit) words it wishes to transfer = 1010H.**
17. **CT8020 checks number of words ready to transfer.**
18. **CT8020 responds with Record S3 = 1000H or 1010H. If number of words is not zero DATAFLAG/ signal is asserted to indicate the beginning of data transfer.**

19. **Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register. This clears the STATUS READY bit.**
20. **If number of words to transfer is zero (S3 = 1000H), Host goes back to step 13.**
21. **Optional: Host waits for DATAFLAG/ signal to be asserted**
22. **Host writes data transfer command = 1000H to Software Control Register**
23. **CT8020 responds with 16-bit data word in Software Status Register**
24. **Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register. This clears the STATUS READY bit.**
25. **Repeat steps 22-24 until all (16) data words are transferred**
26. **CT8020 de-asserts DATAFLAG/ signal to indicate the end of data transfer**
27. **Optional: Host waits for DATAFLAG/ to be de-asserted**
28. **Repeat steps 13-27 until recording finished**
29. To end recording host writes IDLE command or Record Stop command and waits for status response.

Note: **bold text** indicates the record software data transfer loop.

9.6.5 Select TrueSpeech/G.723.1 Record Rate

This command allows the host to select the TrueSpeech data rate used in compressed record mode. The available rates are: 8.5, 6.3, 5.3, 4.8 and 4.1 Kbps. This command should be issued prior to starting record using the RECORD command. The TrueSpeech Record Rate remains in effect until the next TrueSpeech Record Rate command.

Command (513XH):

0101	0001	0011	RATE
(15-12)	(11-8)	(7-4)	(3-0)

Status (513XH):

0101	0001	0011	RATE
(15-12)	(11-8)	(7-4)	(3-0)

RATE	TrueSpeech Compression Rate	Frame Size (16-bit words)
0	8.5 (default)	16
1	6.3 (G.723.1)	12
2	5.3 (G.723.1)	10
3	4.8	9
4	4.1	8
5-15	Reserved	

The Frame Size value indicates the number of 16-bit words in a compressed speech frame for each coding rate. When any of the TrueSpeech compression rates are selected, the frame size is always 16 words or less. Since the size of the CT8020 hardware buffer within the Host port is 16 words, the Host can "burst" read the complete speech frame of 16-8 words without needing to check the RX Ready bit before each individual word is read.

9.6.6 Enable VAD

The G.723.1 / TrueSpeech 6.3, 5.3, 4.8 and 4.1 rates support VAD (Voice Activity Detection) and CNG (comfort noise generation) as defined in the ITU-T G.723.1 Annex A specification. This provides a form of built-in "silence compression". On the speech encode (record) side the VAD feature can be selectively enabled or disabled. On the decode (playback) side, generation of "comfort noise" CNG is automatic and is triggered by specially formatted speech frames that are generated by the encoder when VAD is enabled. By default, the encoder VAD is disabled.

Note that the size of the physical data transfer performed for each speech frame when reading or writing to the CT8020 is determined by the initial speech mode selection. For example if the record session is started in 6.3 mode, then all data transfers will consist of 12 word frames. The VAD/CNG frames which contain a smaller amount of significant data (2 words or 2 bits) have the unused portions of the frame padded with zeros.

To enable VAD:

Command   513FH
Status   513FH

To disable VAD:

Command   513EH
Status   513EH

9.6.7 Switching between TrueSpeech/G.723.1 6.3 and 5.3

The CT8020 supports on-the-fly switching between the TrueSpeech 6.3 and 5.3 data rates as required by the ITU G.723.1 specification. To enable switching between these two rates, the RECORD operation **must** be started with the 6.3 rate selected. This sets the frames size used for CT8020-to-Host transfer to 12 words. When dynamically switching between the 6.3 and 5.3 rates the frames size remains fixed throughout the record process. The 12 word frame size It is used for both the 6.3 **and** 5.3 speech data frames, even though the 5.3 speech frame only contains 10 words. This prevents synchronization problems between the time at which the compression rate is changed and the time at which the compressed data is read out from the CT8020. When a 5.3 frame is read from the CT8020s Hardware Receive Buffers after on-the-fly switching from the 6.3 rate, the Host must read 12 words instead of 10. In this case the last two words of data may be discarded.

Switching between the 6.3 and 5.3 rates is performed using the Select TrueSpeech Record Rate command (above). To support on-the-fly switching, the CT8020 will accept this command after the record process has been started. If the CT8020 is instructed to make an unsupported rate switch (for example between TrueSpeech 6.3 and TrueSpeech 8.5), the status response from the Select TrueSpeech Record Rate will be zero, and the CT8020 record operation will continue to operate with the old TrueSpeech rate.

The l.s two bits of the first data word of a G.723.1 6.3 or 5.3 speech frame are encoded to indicate the speech frame type.

During Playback (de-compression) the CT8020 will test the two l.s. significant control bits only when the current host selected TrueSpeech rate is 6.3 or 5.3. In this case, the CT8020 will automatically perform the correct decoding of the speech frames independently of which rate is selected by the host . To support on-the-fly switching for Playback, Playback must be started with the 6.3 rate selected. This fixes the frame size used for Host-to-CT8020 transfer at 12 words. When transferring a 5.3 speech frame into the CT8020 when the 6.3 rate was initially selected, the Host should append two dummy words (zeros) at the end of the 10 word TrueSpeech 5.3 frame.

To switch between other speech rates, the Host must stop and re-start playback/record. The Host is responsible for synchronizing the rate switch between playback and record sources.

9.6.8 G.723.1 Frame Type Encoding

The least significant two bits of the first word of the TrueSpeech 6.3 and 5.3 frames are defined by the ITU-T G.723.1 v5.1 (final formal release) specification to indicate the speech data rate as shown:

Bit 1-0	Frame Type	Data Rate	Number of significant data words
00	0	TrueSpeech 6.3 data frame (12 words)	12
01	1	TrueSpeech 5.3 data frame (10 words)	10
10	2	Silence / Comfort Noise Generation frame (only first 2 words contain useful data). All other data words are set to zero	2
11	3	Repeat last CNG frame (only l.s. 2 bits of first data word are used). All other data words are set to zero	2 bits

Note that the Bit 1-0 encoding is different from that used in previous firmware versions of the CT8020 which implemented pre-release versions of G.723.1, (firmware revisions 0109 and 0112)

The Host can examine these two bits to distinguish between 6.3 and 5.3 frames (only) to determine the data rate and the number of valid data words in the frame. This bit encoding applies **only** to the 6.3 and 5.3 TrueSpeech frames. There is no bit encoding provided for the 8.5, 4.8 and 4.1 rates.

When implementing a real-time digital compressed speech link, the host and data transport service should be able to transfer all four types of speech frame end-to-end. The host may take advantage of the smaller effective frame size of the silence frames by using the unused portion of the frame for transporting non-speech data. However, before writing the silence frames to the decoder, the host should restore the unused portions of the silence frames to zero.

The CT8020 implements additional non-standard frame encodings as follows:

1. A speech frame which consists of all zeros will be interpreted as an instruction to the playback channel to output pure silence for one frame period. This applies to all TrueSpeech rates, including 8.5, 6.3, 5.3, 4.8 and 4.1.
2. A speech frame which has the first two data words set to FFFFH, with the remaining words set to all zeros, will be interpreted as an instruction to activate the G.723.1 frame erasure mechanism. This should be used where the host needs to instruct the CT8020 playback channel to replace a dropped or corrupt speech frame by extrapolating speech data from previous speech frames. This feature is available only with the TrueSpeech 6.3, 5.3, 4.8 and 4.1 data rates.

When reading or writing speech frames, to or from the CT8020, the number of physical words transferred for each individual frame is fixed during each record/playback session. For example, if the record/playback session is started in 6.3 mode, then all frames will contain 12 words. Frames which use less than this number of words for actual data will have the unused portion of the frame set to zero. This approach simplifies the coding of low level driver software such that it does not need to deal with variable sized data frames. This is particularly significant when dealing with DMA type transfer.

9.6.9 Programming the Record Peak Threshold

The PEAK bit in the Record mode status S2 response can be used by the host to implement silence detection during record. The PEAK bit is set whenever the average signal level for the most recent record frame is greater than the Input Peak Threshold. Although the CT8020 includes a record data frame buffer which can hold a number of record data frames, the PEAK indication provided always refers to the most recent frame recorded. In most cases, where the host services the CT8020 record data frame buffer every frame period (30 ms), there should never be more than one data frame in the buffer. The signal level measured is the input signal level before any scaling occurs due to the Record Volume Control or AGC.

Command C1 (CF99H):

1100 1111 1001 1	001
(15-3)	(2-0)

Status S1:

1100 1111 1001 1	001
(15-3)	(2-0)

Command C2:

Threshold Value
(15-0)

Status S2:

Threshold Value
(15-0)

By default, the Threshold Value is set to 0100H.

9.6.10 Reading the Record Level Value and Threshold Value

The Threshold Value programmed, together with the actual current frame average Level Value can be read using the command:

Command (CF88H or CF89H):

1100 1111 1000 1	00X
(15-3)	(2-0)

Status:

Threshold or Level Value
(15-0)

Where   X = 0   selects reading the Level Value.
         X = 1   selects reading the Threshold Value.

The level value is calculated using the following algorithm:

LEVEL = 0

FOR each of 240 INPUT samples per frame
        IF INPUT < 0 THEN INPUT = -1 * INPUT
        LEVEL = LEVEL + INPUT

LEVEL = LEVEL / 256

Note that this is an average signal level (not r.m.s.). The division by 256 instead of 240 leads to a slight understatement of the true average level. The fractional error is 240/256 = 0.9375, or 6.25%. Dividing by 256 instead of 240 requires less processing by the CT8020 device.

Threshold Level Scale

The threshold level scale is relative to the maximum positive full scale value of 7FFFH (decimal 32767). This corresponds to an input signal level of approximately + 3dBm0 from the external mu-law codec.

The precise input signal level scale can be calculated thus:

Input Level in dBm0 = +3.17 - 20 log(base 10) ((input level/32767) * 256/240)

so the default threshold level of 0100H = 256 decimal, corresponds to -38.4 dBm0.

To calculate the actual average input signal level, read the LEVEL from the device and then perform the following calculation:

CORRECTED LEVEL = (LEVEL * 256) / 240

input level in dBm0 = 3.17 - 20 * log10(CORRECTED LEVEL / 32767)

9.7 PLAYBACK

Command (C1 = 2CXXH):

0010	11	000	PLAYMODE	00	TFR Mode
(15-12)	(11-10)	(9-7)	(6-4)	(3-2)	(1-0)

Status (S1):

0010	11	000	PLAYMODE	00	TFR Mode
(15-12)	(11-10)	(9-7)	(6-4)	(3-2)	(1-0)

9.7.1 Transfer Mode

The TFR Mode field is used to select the mode of data transfer used:

TFR Mode	Data Transfer Mode
00	Data Transfer via Software Command and Status Registers (CT8015/CT8005 protocol mode). See section on Host Data Transfer Modes and Record Protocol.
01	Equivalent to TFR Mode 11, with the addition that data frame alignment is strictly maintained. See section called Playback Frame Alignment Using Transmit Data Buffer for more details. This is a new feature introduced with firmware revision 0114 in the CT8020D11AQC part.
10	Reserved
11	Data Transfer via Host Transmit Data Buffer Access Port. Poll Sync Mode should be selected when using this data transfer option. This data transfer mode must be selected if performing DMA transfers using the TXDREQ and TXDACKN signals. See section on Host Data Transfer Modes and Record Protocol.

For new designs using TFR Mode = [binary] 11 or 01 is recommended.

The **C2-S2**, **C3-S3** commands detailed below are used once at the beginning of playback if TFR Mode = [binary] 11 or 01. If TFR Mode = 00, the C2-S2, C3-S3 commands are used to transfer playback speech data via the Software Control and Status Register.

The Data Transfer command is required only if TFR Mode = 00 (CT8015 / CT8005 protocol mode). This command is used only if transferring speech data via the Software Control and Status Registers.

See section on Playback Protocol.

Command (C2 = 2000H):

0010	0000	0000	0000
(15-12)	(11-8)	(7-4)	(3-0)

Status (S2):

0001	F3	F2	F1	F0	0	0	DTMF VALID	CPF VALID	DTMF DIGIT
(15-12)	(11)	(10)	(9)	(8)	(7)	(6)	(5)	(4)	(3-0)

For information on CPF F3-0 and DTMF detection please refer to section on Line Monitoring.

Command (C3= 20XXH):

0010	0000	REQUEST NUMBER OF WORDS TO TRANSFER
(15-12)	(11-8)	(7-0)

Status (S3):

0010	0	0	00	**ACTUAL** NUMBER OF WORDS TO TRANSFER
(15-12)	(11)	(10)	(9-8)	(7-0)

Data Transfer Command:

16-bit speech data word
(15-0)

Data Transfer Status:

16-bit speech data word
(15-0)

9.7.2 Playback Modes

PLAYMODE	Frame Size (words)	Playback Modes
000	16-8	TrueSpeech at 8.5, 6.3, 5.3, 4.8 or 4.1 Kbits/sec - See Select TrueSpeech Playback Rate command.
001		Reserved
010	120	64 Kbit/sec A-law / Mu-law PCM (120 words per 30ms data frame)
011		Reserved
100	120	64 Kbits/sec 8-bit signed linear (120 words per 30 ms data frame)
101	120	64 Kbits/sec 8-bit unsigned linear (120 words per 30 ms data frame)
110	240	128 Kbits/sec 16-bit signed linear (240 words per 30 ms data frame)
111		Reserved

Notes:
1. All data rates assume that the codec connected to the CT8020 operates at 8000 samples/sec
2. The 30 ms frame interval is based on counting 240 samples from the codec.
3. Mode 010, PCM mu-law is a "pass through mode", where the data from the host is passed to the codec entirely unmodified, (provided that the playback volume is set to 0100H).

4. 16 bit linear data is signed integer (2's complement form), positive full scale is 7FFFH, negative full scale is 8000H, zero is 0000H

5. 8 bit linear data is signed byte (2's complement form), positive full scale is 7FH, negative full scale is 80H, zero is 00H

6. 8 bit linear WSS data is unsigned byte, positive full scale is FFH, negative full scale is 00H, zero is 80H. This is the format used for 8-bit WAVE format data (Windows Sound System). Data can be converted between the two 8-bit formats by simply inverting the ms bit.

7. The TrueSpeech rate 8.5,6.3,5.3,4.8 or 4.1 is selected using the Select TrueSpeech Playback Rate command.

8.   Selection between A-law / Mu-law is made using the codec configuration command. With an external Mu-law codec configured, RECMODE = 100 selects Mu-law data. With an external A-law codec configured, RECMODE = 100 selects A-law data.

9.7.3 Playback Protocol

Example 1 : TrueSpeech 6.3 Playback via Host Transmit Data Buffer Access Port - Host Polling

This example shows how to start playback using TrueSpeech 6.3 with data transfers performed via the Host Transmit Data Buffer Access Port. All data transfers in this example are performed by the Host controller. The Host polls the Hardware Status Register to perform data synchronization.

Starting Playback

1. CT8020 is in IDLE or RECORD state.
2. Host checks for CONTROL READY state in Hardware Status Register.
3. Host selects TrueSpeech 6.3 playback by writing the Select TrueSpeech Playback Rate command = 5231H to the Software Control Register.
4. CT8020 responds via the Software Status Register.
5. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register. This clears the STATUS READY bit.
6. Host selects Poll Sync Mode for playback using the command 5202H.
7. CT8020 responds via the Software Status Register.
8. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register. This clears the STATUS READY bit.
9. Host selects Playback by issuing the PLAYBACK "C1" command = 2C03H via the Software Control Register. This also informs the CT8020 that data transfers will occur via the Host Transmit Data Buffer Access Port (TFR Mode = [binary] 11).
10. CT8020 responds via the Software Status Register.
11. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register S1 = 2C03H. This clears the STATUS READY bit.
12. Host writes PLAYBACK "C2" command = 2000H to the Software Control Register.
13. CT8020 responds via the Software Status Register.
14. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register S2 = 2000H. This clears the STATUS READY bit.
15. Host writes PLAYBACK "C3" command = 200CH to the Software Control Register. This command includes the requested number of words per frame to transfer. In this case (TrueSpeech 6.3) this is 12 = 0CH.
16. CT8020 responds via the Software Status Register.
17. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register S3 = 200CH. This clears the STATUS READY bit.

The CT8020 is now in playback mode. The CT8020 will be ready to consume a compressed speech frame every 30 ms. The following sequence is used to transfer each compressed speech frame from the Host to the CT8020:

1. Host waits for TX Ready bit to be set in the Hardware Status Register
2. Host writes 12 words (for TrueSpeech 6.3) to the Host Transmit Data Buffer Access Port.

The CT8020 includes 240 words (480 bytes) of internal buffering. This is sufficient storage space for 20 TrueSpeech 6.3 speech data frames (600 ms). At the start of playback, the CT8020 will keep re-asserting the TX Ready condition until the internal 480 byte buffer is full, and the CT8020 has "pre-fetched" 20 frames. If the host needs to reduce the number of speech data frames "pre-fetched" by the CT8020, it can do so using the playback Set Buffer Depth command (528XH). This can be set so as to reduce the effective size of the internal buffer.

To terminate playback:

1. Host writes IDLE = 0000H command or STOP PLAYBACK = 5220H command to the Software Control Register.
2. CT8020 terminates playback, discards data in its internal playback buffer, and clears TX Ready if set (in the Hardware Status Register).
3. CT8020 writes status response to the Software Status Register.
4. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register. This clears the STATUS READY bit.

When the IDLE of STOP PLAYBACK command is used to terminate playback, the CT8020 will discard data in its internal playback buffer. In some cases, this may not be the desired behavior. For example, when playing back TrueSpeech 6.3 data stored in a disk file, if the IDLE or STOP PLAYBACK command is issued immediately on encountering end-of-file (EOF), then the last 20 frames (600 ms) of the message will not be played. The Host may wish to make use of the playback Buffer Monitoring command (5212H). Using this command, the Host can poll the CT8020 and wait until all the internally stored speech data has been played out before issuing the IDLE or STOP PLAYBACK command.

Note that after writing the IDLE or STOP PLAYBACK command to terminate playback, the host should not attempt to access the Host Transmit Data Buffer Access Port even if the TX Ready bit is set.

Example 2 : TrueSpeech 5.3 Playback via Host Receive Data Buffer Access Port - Host Interrupt

This example shows how to start playback using TrueSpeech 5.3 with data transfers performed via the Host Transmit Data Buffer Access Port. All data transfers in this example are performed by the host controller. The Host uses an interrupt service routine (ISR) to perform data transfer.

Starting Playback

1. CT8020 is in IDLE state or RECORD.
2. Host checks for CONTROL READY state in Hardware Status Register.
3. Host selects TrueSpeech 5.3 playback by writing the Select TrueSpeech Playback Rate command = 5232H to the Software Control Register.
4. CT8020 responds via the Software Status Register
5. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register. This clears the STATUS READY bit.
6. Host selects Poll Sync Mode for playback using the command 5202H.
7. CT8020 responds via the Software Status Register.
8. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register. This clears the STATUS READY bit.
9. Host selects Playback by issuing the PLAYBACK "C1" command = 2C03H via the Software Control Register. This also informs the CT8020 that data transfers will occur via the Host Transmit Data Buffer Access Port (TFR Mode = [binary] 11).
10. CT8020 responds via the Software Status Register.
11. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register S1 = 2C03H. This clears the STATUS READY bit.
12. Host writes PLAYBACK "C2" command = 2000H to the Software Control Register.
13. CT8020 responds via the Software Status Register.
14. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register S2 = 2000H. This clears the STATUS READY bit.
15. Host writes PLAYBACK "C3" command = 200AH to the Software Control Register. This command includes the requested number of words per frame to transfer. In this case (TrueSpeech 5.3) this is 10 = 0AH.
16. CT8020 responds via the Software Status Register.
17. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register S3 = 200AH. This clears the STATUS READY bit.

18. Host sets up an ISR to service interrupts from the CT8020.
19. Host programs the Hardware Control Register to generate an interrupt from the CT8020 on the TX Ready condition by writing 0402H (Master Enable set, TX Ready IE set).

The CT8020 is now in playback mode. The CT8020 will consume a compressed speech frame every 30 ms. The following sequence is used by the Host ISR to transfer each compressed speech data frame from the Host to the CT8020:

1. Host gets interrupt from CT8020 (optionally checks that TX Ready is set).
2. Host writes 10 words (for TrueSpeech 5.3) into the Host Transmit Data Buffer Access Port.

The CT8020 includes 240 words (480 bytes) of internal buffering. This is sufficient storage space for 24 TrueSpeech 5.3 speech data frames (720 ms). At the start of playback, the CT8020 will keep re-asserting the TX Ready condition until the internal 480 byte buffer is full, and the CT8020 has "pre-fetched" 24 frames. If the host needs to reduce the number of speech data frames "pre-fetched" by the CT8020, it can do so using the playback Set Buffer Depth command (528XH). This can be set so as to reduce the effective size of the internal buffer.

To terminate playback:

1. Host disables interrupts from the CT8020 by writing 0000H to the Hardware Control Register.
2. Host writes IDLE = 0000H command or STOP PLAYBACK = 5220H command to the Software Control Register.
3. CT8020 terminates playback, discards data in its internal playback buffer and clears TX Ready if set (in Hardware Status Register).
4. CT8020 writes status response to Software Status Register.
5. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register. This clears the STATUS READY bit.

Note that after writing the IDLE or STOP PLAYBACK command to terminate playback, the host should not attempt to access the Host Transmit Data Buffer Access Port even if the TX Ready bit is set.

When the IDLE of STOP PLAYBACK command is used to terminate playback, the CT8020 will discard data in its internal playback buffer. In some cases, this may not be the desired behavior. For example, when playing back TrueSpeech 5.3 data stored in a disk file, if the IDLE or STOP PLAYBACK command is issued immediately on encountering end-of-file (EOF), then the last 24 frames (720 ms) of the message will not be played. The Host may wish to make use of the playback Buffer Monitoring command (5212H). Using this command, the Host can poll the CT8020 and wait until all the internally stored speech data has been played out before issuing the IDLE or STOP PLAYBACK command.

Example 3 : Linear 16-bit Playback via Host Transmit Data Buffer Access Port - Using DMA

This example shows how to start playback in uncompressed 16-bit Linear format speech with data transfers performed via the Host Transmit Data Buffer Access Port. All data transfers in this example are performed by an external DMA controller.

Starting Playback

1. CT8020 is in IDLE state or RECORD state.
2. Host checks for CONTROL READY state in Hardware Status Register.
3. Host selects Poll Sync Mode for playback using the command 5202H.
4. CT8020 responds via the Software Status Register.
5. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register. This clears the STATUS READY bit.
6. Host selects Playback by issuing the PLAYBACK "C1" command = 2C63H (PLAYMODE = [binary] 110) via the Software Control Register. This also informs the CT8020 that data transfers will occur via the Host Transmit Data Buffer Access Port (TFR Mode = [binary] 11).
7. CT8020 responds via the Software Status Register.
8. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register S1 = 2C63H. This clears the STATUS READY bit.
9. Host writes PLAYBACK "C2" command = 2000H to the Software Control Register.
10. CT8020 responds via the Software Status Register.
11. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register S2 = 2000H. This clears the STATUS READY bit.
12. Host writes PLAYBACK "C3" command = 20F0H to the Software Control Register. This command includes the requested number of words per frame to transfer. In this case (uncompressed 16-bit linear) this is 240 = F0H.
13. CT8020 responds via the Software Status Register.
14. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register S3 = 2000H. This clears the STATUS READY bit. The S3 response sets the actual number of words to transfer to 00H. This transfer count indicates the number of words to be transferred via the Software Control and Status Registers. Since this example uses TFR Mode = [binary] 11, no data is transferred via the Software Control and Status Registers, instead the data transfer takes place via the Host Transmit Data Buffer Access Port.
15. Host programs external DMA controller to accept DMA requests from the CT8020 (See DMA Direction bit in Hardware Control Register). Host configures a data buffer in the Host memory to store the speech data ready for DMA. The DMA memory buffer should be an integral multiple of the speech frame size. In the case of uncompressed 16-bit Linear, this should be N*480 (bytes).
16. Host sets up an ISR to handle an end-of-transfer (EOT) interrupt from the DMA controller when it reaches the end of the DMA buffer. Alternatively, if the DMA supports circular-buffering (auto-initialize), the Host can poll the DMA to determine when the end of the buffer is reached.
17. Host programs the Hardware Control Register to generate a DMA request from the CT8020 on the TX Ready condition by writing 00A0H (TX DMA Burst Mode, TX DMA enable) - or 01A0H (TX DMA Burst Mode, TX DMA enable, DMA Direction bit set).

The CT8020 is now in playback mode. The CT8020 will consume an uncompressed speech frame every 30 ms. The following sequence occurs between the CT8020 and the DMA controller to transfer data:

1. CT8020 is ready to receive 240 words (480 bytes) of uncompressed 16-bit speech data.
2. CT8020 asserts TX Ready.
3. TX Ready drives TXDREQ.
4. DMA controller responds to TXDREQ by asserting TXDACKN.
5. DMA controller performs a burst transfer of 16 words (32 bytes) from the Host DMA memory buffer to the CT8020.
6. CT8020 de-asserts TX Ready.

7. CT8020 transfers 16 words from the Host Transmit Data Buffer into its internal playback buffer.
8. Repeat 2-7 until all 240 words of the speech data frame have been transferred.

The Host processor also needs to supervise the operation of the DMA controller and arrange for the re-filling of the DMA buffer during playback (e.g. read from disk). When the DMA controller reaches the end of the DMA buffer, the Host must re-fill the data (read from disk). The Host can either arrange to receive an EOT interrupt from the DMA controller, or can periodically poll the DMA's internal transfer count register to determine the status of the DMA.

To terminate playback:

1. Host disables DMA requests from the CT8020 by writing 0000H to the Hardware Control Register.
2. Host writes IDLE = 0000H command or STOP PLAYBACK = 5220H command to the Software Control Register.
3. CT8020 terminates playback and clears TX Ready if set (in Hardware Status Register).
4. CT8020 writes status response to Software Status Register.
5. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register. This clears the STATUS READY bit.

Note that after writing the IDLE or STOP PLAYBACK command to terminate playback, the host/DMA should not attempt to access the Host Transmit Data Buffer Access Port even if the TX Ready bit is set.

Example 4: TrueSpeech 8.5 Playback using CT8005/CT8015 protocol via Software Control and Status Registers.

This example shows how to perform TrueSpeech 8.5 playback with TFR Mode = 00 using the CT8015 compatible protocol. Data is transferred via the Software Control and Status Registers. All data transfers are performed by the Host processor. The example shown uses the CT8015 Poll Sync Mode.

1. CT8020 is in IDLE or PLAYBACK state.
2. Host checks for CONTROL READY state in Hardware Status Register.
3. Host selects TrueSpeech 8.5 playback by writing the Select TrueSpeech Playback Rate command = 5230H to the Software Control Register.
4. CT8020 responds via the Software Status Register
5. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register. This clears the STATUS READY bit.
6. Host selects Poll Sync Mode for playback using the command 5202H.
7. CT8020 responds via the Software Status Register.
8. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register. This clears the STATUS READY bit.
9. Host writes Playback C1 command = 2C00H (TrueSpeech 8.5) to the Software Control Register.
10. CT8020 activates playback mode and performs internal synchronizations (1-2 frame delay) .
11. CT8020 responds with Playback status S1 = 2C00H.
12. Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register. This clears the STATUS READY bit.
13. **Host sends Playback C2 command = 2000H.**
14. **CT8020 responds with Playback S2 status = 2000H.**
15. **Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register. This clears the STATUS READY bit.**
16. **Host sends Playback C3 with the number of (16 bit) words it wishes to transfer = 2010H. For TrueSpeech 8.5 the requested transfer count should be 16 = 10H.**
17. **CT8020 checks number of words it is able ready to transfer.**
18. **CT8020 responds with Playback S3 = 2000H or 2010H. If number of words is not zero DATAFLAG/ signal is asserted to indicate the beginning of data transfer.**

19. **Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register. This clears the STATUS READY bit.**
20. **If number of words to transfer is zero (S3 = 2000H), Host goes back to step 13.**
21. **Optional: Host waits for DATAFLAG/ signal to be asserted**
22. **Host writes 16-bit data word to Software Control Register**
23. **CT8020 responds by echoing the 16-bit data word in Software Status Register**
24. **Host waits for STATUS READY indication in the Hardware Status Register, then reads the CT8020 response from the Software Status Register. This clears the STATUS READY bit.**
25. **Repeat steps 22-24 until all (16) data words are transferred**
26. **CT8020 de-asserts DATAFLAG/ signal to indicate the end of data transfer**
27. **Optional: Host waits for DATAFLAG/ to be de-asserted**
28. **Repeat steps 13-27 until playback finished**
29. To end playback host writes IDLE command or Playback Stop command and waits for status response.

Note: **bold text** indicates the playback software data transfer loop.

9.7.4 Playback Frame Alignment Using Transmit Data Buffer

CT8020 firmware revision 0114 (CT8020D11AQC) provides an additional TFR_MODE = 01 [binary] which maintains strict 30ms data frame alignment for all playback rates. The following section describes non-frame-aligned playback using TFR_MODE = 11 [binary]

If performing Playback via the Transmit Data Buffer with TFR_MODE = 11 [binary], the following should be noted:

When the CT8020 completes the transfer of a speech data frame from the Transmit Data Buffer into its playback queue (in the external data SRAM), the CT8020 immediately returns the (empty) Transmit Data Buffer to the host and grants the host access to this buffer. This causes the TX READY signal (and interrupt) to be re-asserted. This happens even when the CT8020s internal memory playback buffer is full.

In the case of **compressed** speech playback (TrueSpeech 8.5 - 4.1), the effect is simply to allow the host to transfer 1 extra compressed speech frame to the CT8020. When the host writes the next compressed speech frame to the CT8020, the CT8020 is unable to empty the Transmit Data Buffer into its internal memory since this memory is full. In this case, the speech data remains in the Transmit Data Buffer until the next 30ms frame period when space becomes available in the internal memory. In this "memory full + transmit data buffer full" state, the TX READY will not be set. This provides an indication to the host that the CT8020 is not ready to accept more data. The effect of all this is to allow the CT8020 to effectively buffer 1 extra frame. This "extra" frame is not included in the frame count returned by the Buffer Monitoring Command.

In the case of **non-compressed** speech, the effect of this behavior is not as simple. With non-compressed playback (16-bit linear, 8-bit linear and 8-bit mu-law/A-law), the empty Transmit Data Buffer is also returned to the host at the end of transfer of each complete speech frame (120 or 240 words). However in this case, the Transmit Data Buffer is not large enough to take the entire next frame. Instead it is able to hold only the first 16 words of the next frame. The result of this is that the frame by frame transfer of data to the CT8020 will occur with a 16 word offset relative to the 120 or 240 word frame boundaries.

For example:

In 16-bit linear playback the 240 word speech frame is broken up into 15 sub-frames of 16 words each for transfer via the Transmit Data Buffer. So the pattern of data transfer, broken down into 30 ms frame periods, will appear as follows:

Playback frame number	Data transferred	Number of sub-frames transferred
1	240 words of frame 1 + 16 words of frame 2	16 (256 words)
2	224 words of frame 2 + 16 words of frame 3	15 (240 words)
3	224 words of frame 3 + 16 words of frame 4	15 (240 words)
Final Frame	224 words of final frame	14 (224 words)

In 8-bit playback (all types), the 120 word speech frame is broken up into 7 sub-frames of 16 words plus 1 sub-frame of 8 words.

Playback frame number	Data transferred	Number of sub-frames transferred
1	120 words of frame 1 (16,16,16,16,16,16,16,8) + 16 words of frame 2 (16)	9 (136 words)
2	104 words of frame 2 (16,16,16,16,16,16,8) + 16 words of frame 3 (16)	8 (120 words)
3	104 words of frame 3 (16,16,16,16,16,16,8) + 16 words of frame 4 (16)	8 (120 words)
Final Frame	104 words of final frame (16,16,16,16,16,16,8)	7 (104 words)

Of particular significance is the sequence of sub-frame sizes transferred by the host to the CT8020 each 30 ms period. For 8-bit playback, the sequence per frame is : 16,16,16,16,16,16,8,16.

In view of this it is recommended that host software performing 8-bit playback should re-check the status of the TX READY bit at least every 8 words transferred to the CT8020.

9.7.5 Select TrueSpeech Playback Rate

This command allows the host to select the TrueSpeech data rate used in compressed playback mode. The available rates are: 8.5, 6.3, 5.3, 4.8 and 4.1 Kbps. This command should be issued prior to starting playback using the PLAYBACK command. The TrueSpeech Playback Rate remains in effect until the next TrueSpeech Playback Rate command.

Command (523XH):

0101	0010	0011	RATE
(15-12)	(11-8)	(7-4)	(3-0)

Status (523XH):

0101	0010	0011	RATE
(15-12)	(11-8)	(7-4)	(3-0)

RATE	TrueSpeech Compression Rate	Frame Size (16-bit words)
0	8.5 (default)	16
1	6.3 (G.723.1)	12
2	5.3 (G.723.1)	10
3	4.8	9
4	4.1	8
5-15	Reserved	

The Frame Size value indicates the number of 16-bit words in a compressed speech frame for each coding rate. When any of the TrueSpeech compression rates are selected, the frame size is always 16 words or less. Since the size of the CT8020 hardware buffer within the Host port is 16 words, the Host can "burst" write the complete speech frame of 16-8 words without needing to check the TX Ready bit before each individual word is read.

The l.s two bits of the first data word of a G.723.1 6.3 or 5.3 speech frame are encoded to indicate the speech frame type.

During Playback (de-compression) the CT8020 will test the two l.s. significant control bits only when the current host selected TrueSpeech rate is 6.3 or 5.3. In this case, the CT8020 will automatically perform the correct decoding of the speech frames independently of which rate is selected by the host . This includes automatic decoding of the G.723.1 CNG (silence) frames. To support on-the-fly switching for Playback, Playback must be started with the 6.3 rate selected. This fixes the frame size used for Host-to-CT8020 transfer at 12 words. When transferring a 5.3 speech frame into the CT8020 when the 6.3 rate was initially selected, the Host should append two dummy words (zeros) at the end of the 10 word TrueSpeech 5.3 frame.

See also section on on-the-fly switching between TrueSpeech 6.3 and 5.3 data rates.

9.7.6 Inserting Silence During Compressed Speech Playback

When the CT8020 is performing playback in any of the TrueSpeech modes (8.5, 6.3, 5.3, 4.8 or 4.1) it will interpret a speech frame that contains all zeros as an instruction to output 30 ms (one frame period) of pure silence.

9.7.7 Activating The G.723.1 Frame Erasure Mechanism

This is a new feature introduced in CT8020D11AQC, firmware revision 0114.

When the CT8020 is performing playback of G.723.1 / TrueSpeech 6.3, 5.3, 4.8 or 4.1 speech frames, it will interpret a speech frames that has the first two words set to FFFFH and the remainder of the speech frame set to all zeros, as an instruction to perform frame erasure. When Frame Erasure is activated, the CT8020 attempts to construct a replacement for a missing speech frame by extrapolation from previous valid speech frames. The sending of a Frame Erasure frame to the CT8020 based upon detection of dropped or corrupted speech frames is the responsibility of the host software and system communication protocol. The G.723.1 speech frames themselves do not include any built-in error detection mechanism.

9.7.8 G.723.1 Comfort Noise Generation (CNG)

This is a new feature introduced in CT8020D11AQC, firmware revision 0114.

In accordance with Annex A of the ITU G.723.1 specification, the CT8020 will automatically decode CNG frames generated by the VAD (Voice Activity Detector) of a G.723.1 encoder. Decoding of CNG frames is based on examination of the l.s. 2 bits of the first data word of each G.723.1 speech frame. The purpose of the VAD/CNG frame in the G.723.1 Annex A specification is to provide approximate reconstruction of the background noise level and energy spectrum during periods of "silence" that occur between periods of active speech.

The least significant two bits of the first word of the TrueSpeech 6.3 and 5.3 frames are defined by the ITU-T G.723.1 v5.1 (final formal release) specification to indicate the speech data rate as shown:

Bit 1-0	Frame Type	Data Rate	Number of significant data words
00	0	TrueSpeech 6.3 data frame (12 words)	12
01	1	TrueSpeech 5.3 data frame (10 words)	10
10	2	Silence / Comfort Noise Generation frame (only first 2 words contain useful data) All other data words are set to zero	2
11	3	Repeat last CNG frame (only l.s. 2 bits of first data word are used) All other data words are set to zero	2 bits

Note that the Bit 1-0 encoding is different from that used in previous firmware versions of the CT8020 which implemented pre-release versions of G.723.1, (firmware revisions 0109 and 0112)

When sending a type 3 frame to the CT8020 playback channel, please note the requirement to distinguish this type of frame from the Frame Erasure frame (FFFF FFFFH). All the unused bits in the type 3 frame should be set to zero. Although the CNG frames require fewer bits for actual transmission, the host is

required to pad the CNG frames with zeros when writing the frame to the CT8020 in order to make the CNG frame size match the size of the normal speech frame. The CNG frame should be in the form: 0000 0003H to avoid confusion with the special FFFF FFFFH frame erasure frame.

When reading or writing speech frames, to or from the CT8020, the number of physical words transferred for each individual frame is fixed during each record/playback session. For example, if the record/playback session is started in 6.3 mode, then all frames will contain 12 words. Frames which use less than this number of words for actual data will have the unused portion of the frame set to zero. This approach simplifies the coding of low level driver software such that it does not need to deal with variable sized data frames. This is particularly significant when dealing with DMA type transfer.

9.8 Stop Record/Playback

Playback and Record can be stopped using the IDLE command. However, this causes both Playback and Record to be stopped. To stop Playback without stopping Record or to stop Record without stopping Playback, the STOP command may be used. There are two stop commands, one for Playback and one for Record:

STOP RECORD:

Command: 5120H

Status: 5120H

STOP PLAYBACK:

Command: 5220H

Status: 5220H

STOP PLAYBACK and flush codec output buffer (immediate stop)

Command: 5221H

Status: 5221H

In PLAYBACK mode, STOP PLAYBACK causes the CT8020 to enter IDLE mode. In FULL DUPLEX speech mode, this command changes the CT8020 state to RECORD.

In RECORD mode, STOP RECORD causes the CT8020 to enter IDLE mode. In FULL DUPLEX speech mode, this command changes the CT8020 state to PLAYBACK.

Use the STOP PLAYBACK with flush option to terminate playback if the record channel remains active after playback has completed.

9.9 PLAYBACK & RECORD VOLUME CONTROL

9.9.1 Read Record/Playback Volume Control Command:

Command: CF00H/CF01H

1100 1111	0000 00	0	INPUT
(15-8)	(7-2)	(1)	(0)

Status:

RECORD/PLAYBACK VOLUME

INPUT: Set to 0, reads current playback (output) volume
                  Set to 1, reads current record (input) volume

9.9.2 Set Record/Playback Volume Control

Command (C1): CF02H/CF03H

1100 1111	0000 00	1	INPUT
(15-8)	(7-2)	(1)	(0)

Status (S1):

1100 1111	0000 00	1	INPUT
(15-8)	(7-2)	(1)	(0)

INPUT: Set to 0, writes playback (output) volume
                  Set to 1, writes record (input) volume

Command (C2):

RECORD/PLAYBACK VOLUME

Status (S2):

RECORD/PLAYBACK VOLUME

The Record/Playback volume is a "Q8" number which is used to scale the input (record) signal or output (playback) signal (see notes below) .

The scaling performed is :

input or output signal multiplied by (RECORD or PLAYBACK VOLUME)/100H.

So that a record/playback volume setting of:

100H   scales the signal by 1.0
200H   scales the signal by 2.0
80H   scales the signal by 0.5

No protection is given against over-scaling, if the multiplication factor times the input signal exceeds 16 bits, overflow (distortion) will occur.

For best audio performance, optimal scaling of the record signal should be performed by external hardware before A-to-D conversion by the codec, such that the full dynamic range of the codec is utilized. Failure to use appropriate external gain will result in increased quantization noise being introduced into the recording. Note however, that excessive external gain may cause problems with correct operation of the Acoustic Echo Cancellor. Also if the AEC feature is used, then the external gains must be fixed.

Do not attempt to use the CT8020 AEC feature with an external hardware AGC or ALC circuit.

Note that the 8 bit PCM mu-law codes produced by the codec, when converted to a linear representation occupy 14 bits (including the sign bit). The CT8020 handles these 14 bit codes using a 16 bit word representation such that the 14 mu-law bits are "left-justified" within the 16 bits. The lower (least significant) two bits are padded with zeros. This ensures compatibility with digital recordings originating from external systems where a full 16 bits of significant input are encoded or compressed. When the CT8020 is used to decode or de-compress such recordings for output to a mu-law codec, the least significant two bits of the de-compressed 16 bit signal are discarded before conversion to mu-law encoding (and output to the codec) takes place. For 8 bit PCM A-law, the linear representation occupies 13 bits. This is also left-justified within 16 bits and the lower bits filled with zeros.

"Q8" format is a notation used to represent fractional numbers. In normal integer arithmetic, it is not possible to represent numbers less than one or any fractional number . To overcome this limitation multiplication by fractional numbers is performed by scaling up the multiplier by a fixed base number and then scaling down the result by the same base number. The base number provides an effective decimal point placed at the base number. That is, when the multiplier equals the base number , the effective multiplication is by 1.0 (multiply by base number, then divide by base number). To keep the scaling down process simple, the number base chosen is always a multiple of 2. This allows scaling down (dividing) by the base to be performed as a simple binary bit-shift. In "Q8" arithmetic, the "decimal point" is placed between bits 8 and 7 of the 16 bit binary multiplier word (l.s. bit is bit 0, ms bit is bit 15). The base number used is 2 to the power 8 or 256 = 100H. So to multiply by 0.5, the Q8 number 80H (= 0.5 * 100H) is used thus : 400H * 0.5 is performed as 400H * 80H / 100H. The divide by 100H is performed not as a division but as a binary 8 bit right shift.

The record and playback volume controls described here do not affect the operation of the CT8020 when in standalone speakerphone mode (analog phone line speakerphone). See Speakerphone mode description for volume control in this mode.

9.9.3 Automatic Gain/Level Control (AGC or ALC)

The CT8020 includes an AGC feature that can be used in record mode for automatic level adjustment when recording messages.

For optimal Acoustic Echo Cancellor (AEC) performance, the Host should make sure that the AGC is switched off before activating the AEC.

The purpose of the Acoustic Echo Cancellor (AEC) is to attenuate, as far as possible, acoustic echoes from the speaker that are picked up by the microphone. The purpose of the Automatic Gain Control (AGC) is to amplify low level signals that are picked up by the microphone. As a result of this, the AGC and AEC tend to operate in conflict with each other.

However, firmware revision 0114 (CT8020D11AQC) incorporates an additional feature the reduces the amount of conflict that exists between the AEC and AGC. In this device version, the AGC includes a feature that reduces that rate of gain increase allowed when the AEC status indicates that the active speech direction is from the far-end talker. If the user requires that the AGC and AEC must operate concurrently, then the following recommendations should be followed:

1. Limit the maximum AGC gain to the lowest value that produces acceptable results.
2. Make use of the hold time feature of the AGC to minimize gain increases during short conversation pauses.
3. Increase the amount of Echo Suppression (loop attenuation) used by the echo cancellor to compensate for the additional gain introduced by the AGC.
4. Activate the "advanced" AEC features.

Activating the AGC, disables the Record Volume Control. The Record Volume Control has no effect when the AGC is active, however, Record Volume Control setting changes are retained by the CT8020 device and will become effective when the AGC is de-activated.
The AGC provides the following parameters which are programmable by the host:

Max Gain: The maximum gain (max amplification) provided by the AGC

Min Gain: The minimum gain (max attenuation) provided by the AGC

Attack Threshold: The AGC output signal level above which attack occurs (gain reduction) in the attack phase and below which decay occurs when in the decay phase (gain increase).

Attack time-constant: This controls the rate at which the gain decreases during the attack phase

Decay time-constant: This controls the rate at which the gain increases during the decay phase.

Hold Time: The length of time that the AGC gain is held constant following the end of the attack phase and before the beginning of the decay phase

Start Gain: The initial gain setting to use when the AGC is activated. This may be set anywhere between the min and max gain values.
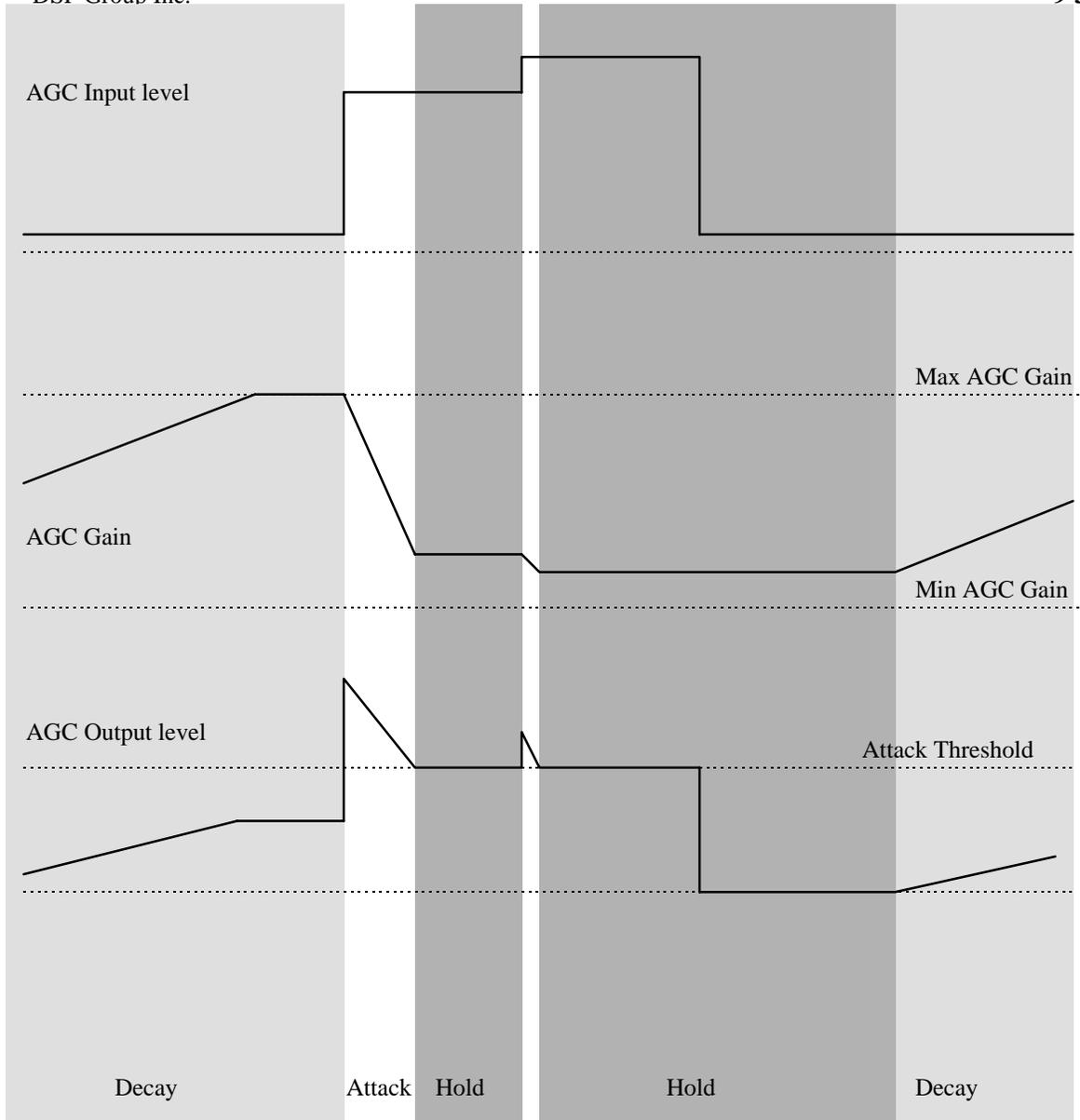
Figure 9-1 AGC Attack Hold & Decay

The figure above, shows the AGC Input signal level (or signal "envelope"), the AGC Gain and the AGC Output signal level.

During the initial Decay phase shown, the input signal is constant at a low level. Since the AGC output level is below the Attack Threshold, the AGC gain increases which in turn increases the output signal level. In this example the gain increases until the AGC Max Gain value is reached, at which point no further increase in gain is possible.

In the next phase, the input signal level suddenly increases, causing the output signal level to exceed the Attack Threshold. At this point the AGC enters the Attack Phase, and the AGC gain is decreased until the output signal level is below the Attack Threshold.

Once the output level is below the Attack Threshold once more, the AGC enters the Hold Phase. In this phase the output level remains at, or below the Attack Threshold. On entering the Hold phase, the AGC sets an internal Hold timer, which then starts to decrement.

Before, the Hold timer can expire, the input signal level increases again, resulting in a second attack phase. After the output level is reduced below the Attack Threshold again, the AGC re-starts the Hold phase.

Next the input signal level is suddenly reduced. Since the AGC is still in the Hold phase, no change in the AGC gain occurs, and the AGC output follows the reduction in input signal level.

When the Hold timer expires, the AGC enters the Decay phase again, and the AGC gain starts to increase.

The rate at which the gain increases during the Decay phase (decay time-constant) and the rate in which the gain reduces during the Attack phase (attack time-constant) are programmable. Best results for speech recording are normally achieved by selecting a fast Attack time-constant (allows rapid gain reduction) and a slow Decay time-constant (allows only slow gain increase). This configuration causes the AGC to primarily respond to the peak speech level, thus providing relative attenuation of any background noise audible during gaps in the speech. If the Hold time is set to 2-3 seconds, the background noise will remain attenuated even during short pauses in the input speech.

9.9.3.1 Programming the AGC

Setting AGC parameters (CF9xH) :

Command C1:

1100 1111 1001 0	SELECTOR
(15-3)	(2-0)

Status S1:

1100 1111 1001 0	SELECTOR
(15-3)	(2-0)

Command C2:

Parameter Value
(15-0)

Status S2:

Parameter Value
(15-0)

Where SELECTOR is defined:

SELECTOR	Parameter Description
000	AGC Min Gain. The 16 bit parameter value used to set the AGC Min Gain is treated as a "Q8" value. That is, the decimal point used to construct the value is considered to be to the right of bit-8. So in Q8 notation, the value 1.00 is represented by the hex number 0100H (decimal 256). The default value for this parameter is 0020H, this represents the fraction 0.125 in Q8 format. So the default min gain is a multiplier factor of 0.125 or one-eighth or approximately -18 dB. The min gain value can also be regarded as the maximum attenuation of the AGC. In this case, the maximum attenuation is by a factor of 8 or approximately +18 dB.
001	AGC Max Gain. The 16 bit parameter value used to set the AGC Min Gain is treated as a "Q8" value (see min gain). The default value for this parameter is 1000H, this represents the fraction 16.0 in Q8 format. So the default max gain is a multiplier factor of 16 or approximately 24 dB. The default max and min gain, give the AGC gain a range from -18 dB to +24 dB which is a range of 42 dB.
010	AGC Start Gain. The 16 bit parameter value used to set the AGC Start Gain is treated as a "Q8" value (see min gain). The default value for this parameter is 0800H, this represents the fraction 8.0 in Q8 format. So the default max gain is a multiplier factor of 8 or approximately +18 dB. Since the default decay time constant is much larger than the default attack time constant, the default start gain is set high. This is because the time taken to reduce the gain (attack) is much less than the time taken to increase the gain (decay). For example if the initial speech level is very high, the gain will be reduced quickly (attack) to adjust to the high input level. If the initial speech level is low, since the decay time constant is large (slow), increasing the gain to amplify the low speech level may take several seconds. Hence starting with a high gain that can be quickly reduced provides the best initial performance.
011	AGC Hold Time. The 16 bit parameter value used to set the AGC Hold time has units of 250 microseconds. The default value of this parameter is 1F40H (8000 decimal) which corresponds to a Hold Time of 2.00 seconds.
100	AGC Attack Time Constant. See time constant table. The default value of this parameter is 0005H.
101	AGC Decay Time Constant. See time constant table. The default value of this parameter is 000DH (14 decimal).
110	AGC Attack Threshold. The AGC Attack Threshold is the AGC output value above which the AGC enters the Attack phase (gain reduction). The default value of this parameter is

	2000H. The value can be set anywhere in the range 0000H to 7FFFH. Note that 7FFFH is the maximum internal (digital) signal level. So a value of 2000H selects AGC attack when the peak signal amplitude is above 0.25 full scale.
111	AGC On/Off. Setting this parameter to 0001H enables AGC operation, setting the parameter to 0000H disables AGC operation. By default the parameter is 0000H with the AGC in the Off state.

Reading AGC parameters (CF8xH):

The AGC parameters programmed can be read back using the command below:

Command:

1100 1111 1000 0	SELECTOR
(15-3)	(2-0)

Status :

Parameter Value
(15-0)

Time Constant Table

Time Constant Parameter	attack/decay fraction per 125 microseconds = $1/2^{(n+1)}$ $U(n+1) = U(n) - U(n) * fraction$	Time Constant in ms (assuming 8 KHz sample rate)
0	0.5	250 us
1	0.25	512 us
2	0.125	1 ms
3	0.0625	2 ms
4	0.03125	4 ms
5	0.015625	8 ms
6	0.0078125	16 ms
7	0.00390625	32 ms
8	0.001953125	64 ms
9	0.0009765625	128 ms
10	0.00048828125	256 ms
11	0.000244140625	512 ms
12	0.0001220703125	1024 ms
13	0.00006103515625	2048 ms
14	0.00003051757813	4096 ms
15	0.00001525878906	8192 ms

In the Attack phase (gain decreases) , the AGC gain is recalculated every codec sample (125 us) such that

AGC gain = AGC gain - ((AGC gain - min AGC gain) * $1/2^{(n+1)}$)

This behaves as an approximately exponential decay from the current instantaneous gain value towards the min AGC value.

In the Decay phase (gain increases), the AGC gain is recalculated every codec sample (125 us) such that:

AGC gain = AGC gain + ((max AGC gain - AGC gain) * $1/2^{(n+1)}$)

This behaves as an approximately exponential decay from the current instantaneous gain value towards the max AGC value.

Note that the time constant, is the time that it takes for an initial value to decay to 1/e of its initial value where e = 2.71828.

9.10 Pre-Scaling of DTMF and Call Progress Filter Input

The CT8020 provides a pre-scalar multiplier which allows independent adjustment to be made to the input signal level that goes to the tone detection sub-system (DTMF and Call Progress Tone Filters). This pre-scaler (input volume) control is separate from the record and playback volume controls.

The pre-scaler setting can be read using the following command:

Command   = CF05H
Status   = pre-scaler value (default is 0040H)

The pre-scaler setting can be written using the following command:

C1 Command   = CF07H
S1 Status   = CF07H

C2 Command   = new pre-scaler setting
S2 Status   = new pre-scaler setting

The default value for the pre-scaler is 0040H, and it acts as a linear scaler. Changing the pre-scaler setting to 0020H will multiply the signal by 0.5 relative to the normal setting.

9.11 HOST SYNC MODES

The playback and record sync modes can be set independently :

RECORD SYNC:

Set CODEC sync mode :	5100H
Status:	5100H
Set DATA sync mode:	5101H
Status:	5101H
Set POLL sync mode:	5102H
Status:	5102H
Set HOST sync mode:	5103H
Status:	5103H

PLAYBACK SYNC:

Set CODEC sync mode :	5200H
Status:	5200H
Set DATA sync mode:	5201H
Status:	5201H
Set POLL sync mode:	5202H
Status:	5202H
Set HOST sync mode:	5203H
Status:	5203H

Notes
1. The sync modes should normally only be changed when the device is in IDLE mode.
2. CODEC sync mode is the default following reset
3. DATA sync mode is selected automatically during Host-to-Host compression or decompression. This sync mode will remain in effect until a new sync mode command is issued. Once Host-to-Host compression has been started (after the C1 command), it is possible to issue another sync mode command in order to change to a different the sync mode.
4. Select POLL sync mode if TFR_MODE = [binary] 11. Use this mode for DMA and if performing data transfers via the Host Transmit/Receive Data Buffer Access Ports.

9.12 PLAYBACK & RECORD BUFFER CONTROL

9.12.1 Monitoring Buffer Depth

The buffer monitoring commands for the record and playback channels return the number of frames currently present in the respective receive and transmit queues. Each frame corresponds to 30 ms of speech. The host uses these commands for buffer management purposes.

RECORD:

Read Buffer Depth Command: 5112H
Status: the number of record frames currently in the receive buffer.

PLAYBACK:

Read Buffer Depth Command: 5212H
Status: the number of playback frames currently in the transmit buffer.

9.12.2 Speech Frame Create

The frame create command creates an additional speech frame in the transmit or receive buffer provided that the buffer is not full. The frame is created by copying the most recent frame in the buffer.

RECORD:

Create Record Frame: 5117H
Status: 0 or 1   The number of frames created. If the buffer is full the status reply will be 0. If the buffer is not full, and the frame can be created, the status reply will be 1.

PLAYBACK:

Create Playback Frame: 5217H
Status: 0 or 1   The number of frames created. If the buffer is full the status reply will be 0. If the buffer is not full, and the frame can be created, the status reply will be 1.

Note that for playback the G.723.1 / TrueSpeech 6.3, 5.3, 4.8 and 4.1 rates include a built-in frame creation mechanism that is activated using a specially encoded speech playback frame. This mechanism allows replacement of a dropped or corrupted speech frame by extrapolation of speech data from previous frames.

9.12.3 Speech Frame Delete

The frame delete command deletes a speech frame from the transmit or receive buffers provided that the buffer is not empty. The status reply indicates the number of frames deleted.

RECORD:

Delete Record Frame:	5116H
Status:	0 or 1 The number of frames deleted. If the buffer is empty at the time this command is called, there will be no frames to delete and the status reply will be 0. If the buffer is not empty, and a frame is deleted, the status reply will be 1.

PLAYBACK:

Delete Playback Frame: 5216H	
Status:	0 or 1 The number of frames deleted. If the buffer is empty at the time this command is called, there will be no frames to delete and the status reply will be 0. If the buffer is not empty, and a frame is deleted, the status reply will be 1.

9.12.4 Playback & Record Buffer Freeze (Pause)

The buffer freeze command stops output from the playback buffer in the playback channel and input to the record buffer in the record channel. The buffer freeze command can be used to implement a pause feature. When the playback channel is paused, it outputs silence to the external codec. Freezing the playback channel can also be used at the start of playback to pre-load the channel with buffers before the actual start of playback. This creates a reservoir of speech frames within the CT8020 which can be used for smoothing out fluctuations in the rate at which speech frames arrive for playback. The state of the CT8020 internal freeze flag bits can be modified in any mode of operation : IDLE, PLAYBACK, RECORD or FULL DUPLEX.

RECORD:

Freeze Record Channel:	5113H
Status:	5113H

Un-Freeze Record Channel:	5114H
Status:	5114H

Read Record Freeze State:	5115H
Status:	0 or 1 The status returns 1 if the channel is currently in the freeze state, 0 otherwise.

PLAYBACK:

Freeze Playback Channel:	5213H
Status:	5213H

Un-Freeze Playback Channel:	5214H
Status:	5214H

Read Playback Freeze State:	5215H

Status: 0 or 1 The status returns 1 if the channel is currently in the freeze state, 0 otherwise.

Revision 0112 of the CT8020 firmware (CT8020A11BQC) fixed a minor bug which caused incorrect operation of the Buffer Freeze command for Playback when the CT8020's internal playback buffer was completely empty. In earlier versions of the CT8020 firmware, the CT8020 would not output silence when Buffer Freeze was activated if the Playback buffer was empty. In this situation, the CT8020 would continuously re-output the most recent two speech frames. Please also refer to the Playback Auto-Repeat feature described later in this document.

9.12.5 Buffer Depth Limit

The buffer depth limit command can be used to limit the number of speech frames held in the playback or record channel buffers. This allows the host to strictly limit the amount of delay and latency that the buffering of speech frames in the CT8020 can add to an end-to-end speech link. At the same time, the CT8020's buffering capability helps to reduce the load on the host processor by permitting more relaxed real-time deadlines in moving data into or out of the CT8020. The CT8020 has 480 bytes available for storage space for each channel (physically located within the external data SRAM). This is sufficient for up to:

1 uncompressed (480 byte) 16-bit linear frame
2 uncompressed (240 byte) 8-bit/A-law/mu-law frames
15 TrueSpeech frames

The CT8020 does not check the buffer limit set by the host, but simply takes as the actual limit the minimum value of the physical buffer capacity and the host programmed limit. For example, in mu-law mode, if the host programs a limit of 10 frames, the limit used will actually be only 2, the physical capacity of the device. In TrueSpeech 8.5 mode, if the host programs a limit of 10 frames, the limit used will be 10 since this is within the physical capacity of the device.

RECORD:

Set Record Channel Limit:	5180H + X	where X is in the range 0 to 15 (decimal)
Status:	5180H + X	
Read Record Channel Limit:	5118H	
Status:	000XH	where X is the limit programmed

PLAYBACK:

Set Playback Channel Limit:	5280H + X	where X is in the range 0 to 15 (decimal)
Status:	5280H + X	
Read Playback Channel Limit:	5218H	
Status:	000XH	where X is the limit programmed

9.12.6 Playback Auto-Repeat

If data under-run occurs during playback, the transmit buffer becomes empty and the CT8020 will default to repeatedly outputting the most recent speech frame up to a (default) limit of 8 times. This behavior is appropriate to "mask" a short 1 or 2 frame period in which playback data is not available. Repeating the most recent frame 1 or 2 times causes the least perceptible break in the continuity of playback. However, if the data under-run condition persists for a longer period of time, the repeated playback of a single frame can cause annoyance to the user. The auto-repeat limit can be programmed by the host in the range 1-15. Programming the auto-repeat limit to zero, will cause auto-repeat to operate continuously. When the auto-repeat limit is exceeded the CT8020 will output silence until more playback data becomes available.

Command: 525XH

Status: 525XH

Where X selects the number of repeats in the range 1 - 15. If X is set to zero, the CT8020 will continuously auto-repeat the most recent frame.

9.13 FULL DUPLEX SPEECH MODE

Full duplex (DSVD) speech mode is the simple combination of PLAYBACK and RECORD operating concurrently (and independently). Full duplex mode is entered by starting both Playback and Record in either order.

If the Host wishes to take advantage of the fact that the record and playback data streams are synchronous within the CT8020, in order to use a single interrupt source for generating an interrupt for both Playback and Record, then the RX READY interrupt should be used. Internally the CT8020 process the Playback data stream before processing the Record data stream. So under normal circumstances, the RX READY (record) indication will be asserted after TX READY (playback). Because of the Playback-then-Record order, at the time the RX READY condition is asserted, the TX READY will normally also be set. At this time the Host can perform data transfers for both TX and RX directions.

The only disadvantage to this approach is the restriction imposed on the Host response time when the CT8020's internal playback buffer is **empty** and the internal DSP is operating at close to 100% load (Full Duplex TrueSpeech 6.3 plus concurrent Acoustic Echo Canceller). In a minimum delay environment, the host may wish to attempt to keep the CT8020's internal buffers in the empty state for as much of the time as possible. Reducing the amount of speech buffered within the CT8020 will keep the end-to-end delay to a minimum. Under these circumstances, the response time of the Host using the RX READY assertion to completion of the Playback data transfer to the CT8020 must be shorter, otherwise Playback data under-run will occur.

The diagram below shows typical CT8020 internal processing activity during one 30 ms frame period.
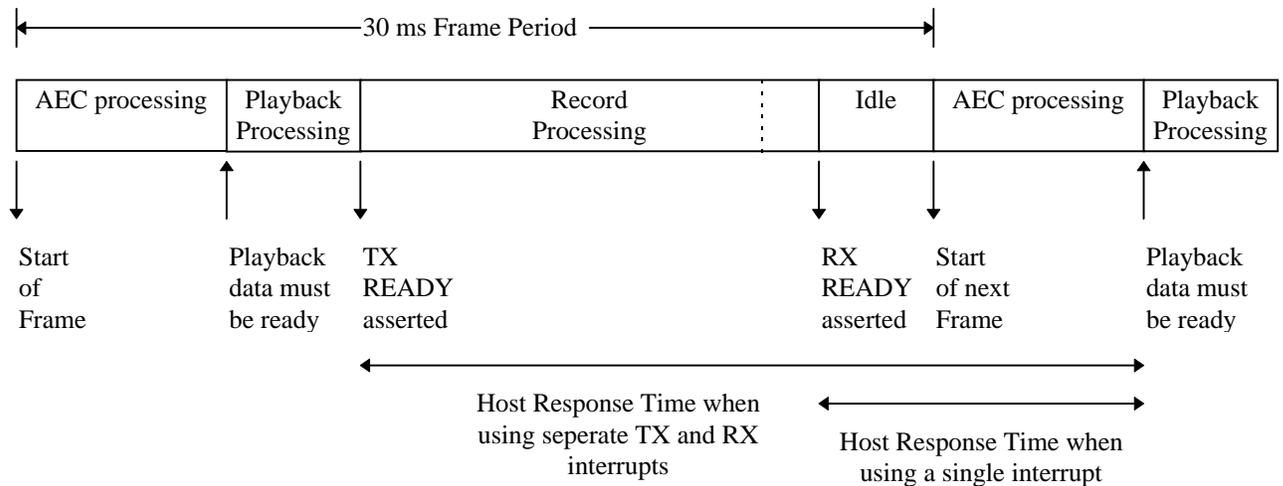
Figure 9-2 CT8020 internal processing activity

The Host Response Time is only an issue if the Host is attempting to implement a **minimum** delay system, where the CT8020's internal buffers are not used to provided additional latency (buffering). If minimum delay is not required, the CT8020's playback buffer can be used to provide extra buffering such that there is always at least 1 speech frame ready and waiting in the playback buffer. In this situation, the Host always has at least a 1 frame period latency in which to respond to the TX READY condition.

9.14 ACOUSTIC ECHO CANCELLOR IN DSVD MODE

The Acoustic Echo Canceller (AEC) may be active only when full duplex (DSVD) speech mode is in operation (except as part of standalone speakerphone mode). For the AEC to function, it requires both an outgoing (playback) and incoming (record) speech data stream for the AEC to operate upon. When the AEC is operating, the Automatic Gain Control (AGC) feature (available in conjunction with record mode) must be de-activated. However, the playback and record level controls are available when the AEC is active. Care must be taken when setting the record and playback levels so as not to compromise operation of the AEC. The purpose of the AEC is to reduce as much as possible, the acoustic echo of the outgoing speech (playback) reflected from the speaker into the microphone (record speech stream). Increasing the playback or record volumes, will increase the level of audible echo.

The AEC is switched on or off using the following commands.

Command:	B001H	AEC on
Status	B001H	
Command:	B002H	AEC off
Status	B002H	

The above commands can be issued at any time, but the AEC will only be active when playback is active (otherwise there is no echo to cancel).

The commands:

Get Speakerphone Status
Set Speakerphone Parameters (speaker and line volume and loop attenuation)
Speakerphone Configuration (loop adjustment mode)

can be used to control the AEC. See the section on (standalone) Speakerphone mode for detailed descriptions of these commands.

The speakerphone commands listed above only work when record and/or playback are active. Sending these commands when the CT8020 is in IDLE mode will cause (improper) entry to standalone speakerphone mode.

Attempting to train the Electrical Echo Canceller (EEC) in DSVD speakerphone mode is not permitted. The EEC is used **only** in standalone speakerphone mode to cancel the electrical signal echo from the telephone line (via the second, optional, codec0).

Use the following sequence of commands (from idle mode)

Start Playback and/or Start Record
AEC on
Set Speakerphone Parameters
optional - Speakerphone Configuration
optional - Get Speakerphone Status

See Appendix A for additional information.

9.14.1 Concurrent AEC and Speech Operation
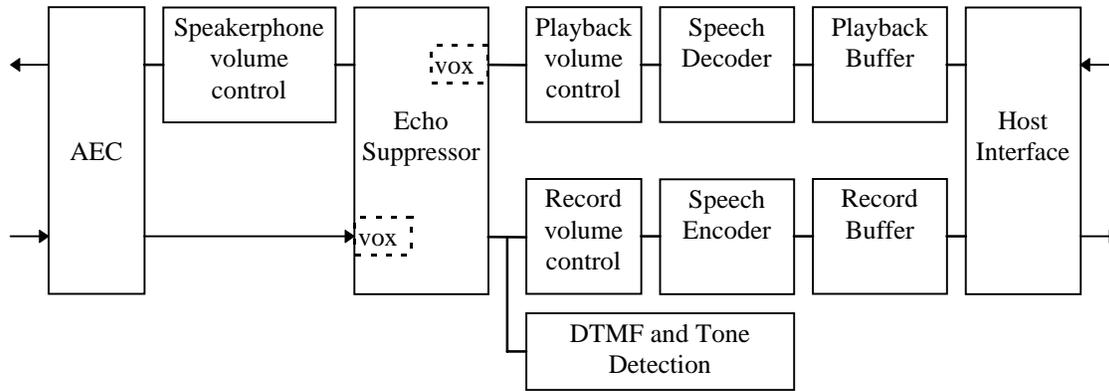
Figure 9-3 AEC and Speech Compression

This diagram shows the relationship of the Speakerphone Acoustic Echo Canceller (AEC) and Echo Suppresser components to the record/playback channels when DSVD speakerphone mode is used.

Note that the speech "direction" decision for the Echo Suppresser is made by the "vox" detectors at the inputs of the Echo Suppresser. Changes to the playback level made using the playback volume control (recommended) will be seen by the "vox" and affect the direction decision. Changes to the playback level made using the Speakerphone volume control (Set Speakerphone Parameters command) will not be seen by the "vox" and will not affect the direction decision.

9.14.2 Activating the Advanced Echo Canceller features in the CT8020

To activate the advanced echo canceller features in the CT8020 use the following command sequence:

Command	Status
E013	E013
0600 or 0C00	0600 or 0C00
E011	E011
0080	0080

These commands may be sent at any time, either before or after the Acoustic Echo Canceller is activated. These commands need only be sent once. They do not need to be sent every time the AEC is started. However, sending these commands multiple times does not cause any problems. The 0C00H option above provides a higher level of echo attenuation.

To de-activate the Advanced AEC features use the following commands:

Command	Status
E013	E013
0000	0000
E011	E011
FFFF	FFFF

Note that these commands are not supported by the CT8020A11AQC chips (engineering samples). Before sending any of these commands to the CT8020, your software should check the revision number of the CT8020 using the 3800H device version command.

Device	Firmware Version
CT8020A11AQC	0109
CT8020A11BQC	0112

9.14.3 Adding Additional Echo Suppression

Additional echo attenuation can be achieved by increasing the level of echo **suppression** used by the CT8020. Echo suppression is different from echo cancellation. In echo cancellation, only the echo component of the input signal is affected, any input signal that originates at the microphone input is not affected. With echo suppression the entire input signal is affected, both the component due to echo and the component due to the "real" microphone input.

Echo suppression was the technique used in traditional half-duplex speakerphones. In this type of phone, only one audio signal direction is enabled at any given time. This takes advantage of the fact that in a normal conversation only one user is talking at any moment. This allows a decision to be made to attenuate one speech direction based on which speech direction is the "in-active" direction. The audio signal for the inactive speech direction is always completely muted. To completely mute one direction of speech, half-duplex speakerphones introduce greater than 60 dB of attenuation into the inactive speech path.. In a half duplex speakerphone, since only one speech direction is enabled at any time, there is no possibility of hearing an echo. The problem with this solution comes when both users attempt to talk at the same time. When this happens the direction decision making logic in the half-duplex speakerphone is unable to function correctly and the result is often that both speech directions are attenuated.

The CT8020 implements a scaleable form of Echo Suppression where the amount of attenuation added to the inactive direction can be programmed in the range 0 to -28 dB. Using 0 dB of echo suppression effectively de-activates the echo suppresser. Providing a scaleable echo suppresser attenuation allows a gradual compromise between full-duplex operation (0 dB suppression) and half-duplex operation (with -28 dB suppression). With a scaleable echo suppresser, even when a speech direction is attenuated, it is not completely muted, so it is possible to tell that speech is present.

By adding a small amount of echo suppression to the CT8020 (around 16 dB), it is possible to ensure that any residual echo not fully canceled by the AEC is removed.

The echo suppression attenuation (loop attenuation) can be programmed only after the AEC is activated and after playback and record has been started. Use the "Set Speakerphone" command described in the speakerphone section of the CT8020 data sheet.

9.14.3.1 Set Echo Suppresser Attenuation

This is the "Set Speakerphone Parameters" command used it standalone speakerphone mode. It may be used in DSVD Speakerphone Mode to set the echo suppresser attenuation. This command should be sent only AFTER starting playback and record.

Command:

1110	001	Line Volume	Speaker Volume	Loop Attenuation
(15-12)	(11-9)	(8-7)	(6-3)	(2-0)

Status:

1110	001	Line Volume	Speaker Volume	Loop Attenuation
(15-12)	(11-9)	(8-7)	(6-3)	(2-0)

Line Volume: This controls the volume transmitted to the telephone line

00	+8 dB
01	+4 dB
10	+0 dB (normal setting)
11	Mute Microphone (also resets AEC)

Speaker Volume: This controls the volume to the speakerphone loudspeaker.

0000	+14 dB
0001	+12 dB
0010	+10 dB
0011	+8 dB
0100	+6 dB
0101	+4 dB
0110	+2 dB
0111	0 dB (normal setting)
1000	-2 dB
1001	-4 dB
1010	-6 dB
1011	-8 dB
1100	-10 dB
1101	-12 dB
1110	-14 dB
1111	Speaker Mute

Loop Attenuation :   Total attenuation used by receive and transmit attenuators
(Echo Suppression)

Full Duplex Operation

000	0 dB
001	-4 dB
010	-8 dB (default for DSVD mode)

Half Duplex Operation

011	-12 dB
100	-16 dB
101	-20 dB
110	-24 dB
111	-28 dB

9.14.4 AEC Train and Lock

This is a new feature introduced with firmware revision 0114 (CT8020D11AQC.

The CT8020 AEC includes features that allow it to be used to cancel fixed non-acoustic echoes. For example, the AEC can be used to cancel electrical echoes created by a 2-to-4 wire telephone hybrid.

When the AEC is used to cancel acoustic echoes, it must cope with real-time changes in the echo path of the acoustic signal. These changes may be caused by movement of the user in front of the speaker and microphone, or by actual physical movement of the speaker or microphone. As a result of this, the AEC must continuously attempt to adapt and search for the optimum echo cancellation setting. The constant search process inevitably means that the AEC may not always be operating at an optimum point.

If the AEC is required to cancel a fixed path electrical echo, it is possible to train the AEC against the fixed path and then lock the AEC training control.

The AEC can be instructed to perform an automatic train-and-lock sequence using the following command:

	Command	Status Response
C1	E012	E012
C2	4004	4004

If the AEC is already in a locked state when this command is set. the AEC is unlocked allowing re-training.

To de-activate the train and lock feature, use the following command sequence:

	Command	Status Response
C1	E012	E012
C2	0004	0004

To force the AEC into a locked state, use the following sequence:

	Command	Status Response
C1	E012	E012
C2	C004	C004

9.14.4.1 AEC Locked State

In the "locked" state, the AEC will not undergo further updates of its internal coefficients unless the amount of instantaneous attenuation measured is greater than the Lock Threshold. This places a significant restriction on the AEC adaptation control algorithm. It is designed to prevent a "hunting" effect where the AEC attempts to adapt to low level noise instead of a real echo signal.

Use of this feature is not recommended for echo paths that can vary in real-time. If the echo path changes while the AEC is in the locked state, the amount of attenuation achieved my never exceed the Lock Threshold. In this situation, the AEC will never update its internal coefficients.

9.14.4.2 Setting the Lock Threshold

The attenuation threshold at which the AEC enters the Locked state is programmable. Use the following command sequence:

	Command	Status Response
C1	E014	E014
C2	XXXX	XXXX

where XXXX is the attenuation threshold in dB.

For example the default threshold is -12 dB and so XXXX = FFF4 (-12 in hexadecimal form)

9.14.4.3 Setting the Un-Lock Threshold

The AEC can be programmed to automatically un-lock if the instantaneous measured attenuation indicates that the AEC is not canceling the echo. This may happen if the echo path is changed.

If the echo path is changed significantly, it is possible that the echo estimate calculated by the AEC is so badly in error that the AEC creates an effect where is INCREASES the echo signal level instead of reducing it. In this situation, the AEC can be programmed to automatically un-lock when amplification of the echo signal is detected:

	Command	Status Response
C1	E01B	E01B
C2	XXXX	XXXX

where XXXX is the attenuation threshold in dB.

For example, the default threshold is +3dB and so XXXX=0003.

Note that when measuring the AEC attenuation, a negative dB value represents a reduction in the output signal level (attenuation), whereas a positive dB value represents an increase in the output signal level (amplification).

9.14.4.4 Freezing the AEC

In the Locked state, the AEC coefficients are updated if the measured attenuation exceeds the Lock Threshold. To cause an complete freeze of the AEC, where no updating of the AEC coefficients take place, simply program the Lock and Un-Lock Thresholds to large values and force the AEC into the locked state.

For example:

	Command	Status Response	
C1	E01B	E01B	program the un-lock threshold to a large
C2	7FFF	7FFF	positive value
C1	E014	E014	program the lock threshold to a large
C2	FF00	FF00	negative value
C1	E012	E012	Force the AEC into the locked state
C2	C004	C004	

9.14.5 Controlling the Automatic Loop Adjustment Attenuation

When the AEC is operating under normal conditions, it constantly monitors the effect of the echo cancellation process. The intent of the AEC is to reduce the amplitude of any echo signals passing through the AEC. When the AEC passes through a signal that originates at the near-end (a signal that is due to the local user talking, not due to an echo of the speaker output), the signal should pass through without any change in amplitude. Under both these sets of conditions, the output signal level from the AEC block should never be larger than the input signal level.

If the AEC detects that the output level of the AEC is greater than the input level of the AEC, this indicates a fault condition. This state may arise if the acoustic echo path is rapidly changed, for example by suddenly moving the microphone to a position immediately in front of the speaker. Under these circumstances, the AEC by default will increase the amount of echo suppression in use to attempt to prevent positive feedback in the audio loop (howling).

9.14.5.1 Programming the Loop Adjustment Threshold

The Loop Adjustment Threshold at which the additional loop attenuation is activated can be programmed by the host:

	Command	Status Response
C1	E01A	E01A
C2	XXXX	XXXX

where XXXX is the Loop Adjustment Threshold in dB.

For example, the default threshold is +1 dB, so XXXX=1dB

The automatic loop adjustment feature can be disabled by programming the Loop Adjustment Threshold to a large positive value, e.g. XXXX=7FFFH or by programming the amount of attenuation added to zero (see below).

Also the automatic loop adjustment feature can be disabled by using the Speakerphone Configuration Command described in the Standalone Speakerphone section. Note that when using the AEC concurrently

with speech compression modes, this particular command can only be sent AFTER enabling the AEC and entering the playback and record states.

9.14.5.2 *Programming the Loop Adjustment Attenuation*

When the AEC detects error-state amplification in excess of the Loop Adjustment Threshold, by default it adds 12dB of echo suppression in addition to the echo suppression (loop attenuation) selected by the Set Echo Suppresser Attenuation command. The maximum amount of total echo suppression in operation is limited to 28dB.

The amount of additional echo suppression introduced can be programmed by the host using the following command:

	Command	Status Response
C1	E015	E015
C2	000X	000X

Where X is between 0 and 7 and represents units of 4dB steps.

For example the default attenuation added is 12 dB, so X=3

When the AEC detects that the error conditions that caused the additional echo suppression to be added no longer exist, the additional echo suppression (loop attenuation) is removed automatically.

9.14.6 **Reading the instantaneous AEC attenuation**

The host can read the approximate instantaneous attenuation as measured internally by the AEC using the following command:

Command   E00A
Status response   XXXX

Where XXXX is the approximate attenuation in dB. This can be a negative value which indicates the current instantaneous echo signal is being attenuated, or a small positive value indicating that either the AEC is not trained, or that no input or echo signal is present. If the attenuation value read is a positive value larger than +6dB, this indicates that the AEC is operating under adverse or error conditions.

The value read can only show a significant negative value (indicating a significant amount of attenuation) when a speaker output signal is present which causes a large input echo. When no input signal is present, the amount of attenuation achieved is indeterminate.

9.14.7 Saving and Restoring the AEC and EEC coefficients

The current AEC and EEC echo estimation filter coefficients can be saved and restored into the external data SRAM attached to the CT8020 device. Coefficients saved in the external SRAMs are never lost except in the case of a power on-off cycle. The coefficients saved are not affected by a device reset. The coefficients will be lost if the external SRAM self test command is used.

The working filter coefficients of the AEC and EEC are reset each time the echo canceller is restarted. In the case of the AEC, the filter coefficients are reset by a AEC-off, AEC-on sequence.

9.14.7.1 Save AEC coefficients

Command   E016
Status   E016

9.14.7.2 Restore AEC Coefficients

Command   E017
Status   E017

9.14.7.3 Save EEC coefficients

Command   E018
Status   E018

9.14.7.4 Restore EEC coefficients

Command   E019
Status   E019

9.14.8 Evaluating Echo Canceller Performance

The CT8020 AEC uses a pair of VOX detectors to detect the presence of speech and control the operation of the echo canceller and echo suppressor. These detectors respond to short term rate of change in signal energy. This enables the detectors to distinguish between real voice activity and back ground noise. As a result of this, it is not appropriate to test the CT8020 AEC performance using continuous sine waves. The CT8020 should only be tested using real speech or alternatively using pulsed sine waves or pulsed white noise. The pulse duration should typically be less than 500 ms.

9.15 SPEECH FRAME INTERRUPT

The CT8020 can provide a speech frame-by-frame interrupt from the TX READY and RX READY signals of the Hardware Status Register. For added flexibility two additional mechanism are provided for generating interrupts derived from the frame rate.

9.15.1 Frame Interrupt via the FR pin

For compatibility with the CT8015, the CT8020 provides a Frame Interrupt signal via the FR/ pin. When record, playback or full-duplex speech mode is active, the FR/ pin is asserted (driven low) every frame period. This makes the FR/ signal useful as a frame interrupt to the host. Since FR/ is asserted every frame period, the host is guaranteed that a new record frame will be available in the receive frame buffer, or a space will be available for a new playback frame in the transmit frame buffer, each time the FR/ is asserted. The host can clear the FR/ signal using the CLEAR FR command:

The FR/ pin is implemented using the GPIO 5 pin. This is an optional signal provided for CT8015 TrueSpeech DSVD Co-Processor compatibility. If this pin is not required, the GPIO 5 pin is available for general purpose use. Instead of using the FR/ pin, the Host can use the IRQN interrupt pin and select that it be driven from the transmit/receive data buffer TX or RX READY signal by programming the Hardware Control Register. This will then provide an interrupt each time a compressed data frame is ready (30 ms). The interrupt is cleared by filling or emptying the data buffer as appropriate.

The following commands are available for controlling the FR/ pin: Enable, Disable, Clear and Read.

Enable FR:

command:	5141H
status:	5141H

by default, the FR pin is enabled.

Disable FR

command:	5142H
status:	5142H

Clear FR

command (5140H)

0101 0001 0100 0000
(15-0)

status:

XXXX XXXX XX	FR	X XXXX
(15-6)	(5)	(4-0)

The state of the FR/ pin (before it is cleared) is returned in bit-5. If the FR pin was asserted prior to being cleared, FR = 0, otherwise FR = 1. The FR/ is active low (when asserted, the pin is low).

Read FR

command (5143H)

0101 0001 0100 0011
(15-0)

Status = YYXXH

YYYY YYYY	GPIO-7	GPIO-6	FRN	X	GPIO-3	GPIO-2	GPIO-1	DATA FLAG
(15-8)	(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)

The state of the FR/ pin is returned in bit-5. If the FR pin is asserted, FR = 0, otherwise FR = 1. The FR/ is active low (when asserted, the pin is low). The state of the FR/ pin is not affected by the Read FR command. See also section on reading and writing the GPIO pins.

9.15.2 Frame Interrupt via Aux Software Status Register

The CT8020 can also be programmed to generate a frame interrupt every N frames via the Aux Software Status Register (ASSR).

Set ASSR update rate:

Command C1   = 5145H
Status S1   = 5145H

Command C2   = N (update ASSR every N frames)
Status S2   = N

If RECORD or PLAYBACK is active, the CT8020 will write its internal frame count to the ASSR every N frames. The Host can then program the CT8020 Hardware Control Register to generate an interrupt on the Aux Status Ready condition. The Host clears the interrupt by reading the ASSR. Setting N to zero, disables update of the ASSR. This is the default setting.

The Host can also read the current value of the internal frame count at any time using the command:

Read Frame Count:

Command   = 5144H
Status   = current frame count.

This frame count is incremented every frame period (30ms) if either RECORD or PLAYBACK is active. The frame counter is cleared on entry to either RECORD or PLAYBACK from IDLE mode.

9.16 DEVICE SELF-TEST

9.16.1 Check Internal Program ROM Integrity

Command = 3000H

0011	00	00 0000 000	0
(15-12)	(11-10)	(9-1)	(0)

Status

0011	X	DATA ROM STATUS	PROGRAM ROM STATUS	X XXXX XXXX
(15-12)	(11)	(10)	(9)	(8-0)

PROGRAM ROM STATUS: Set to 0 to indicate internal program rom checksum is valid.
                             Set to 1 to indicate internal program rom failure.

DATA ROM STATUS: Set to 0 to indicate internal data rom checksum is valid.
                             Set to 1 to indicate internal data rom failure.

X: Reserved bits

9.16.2 Test External Data SRAM

Command = 3001H

0011	00	00 0000 000	1
(15-12)	(11-10)	(9-1)	(0)

Status

0011	SRAM TEST	XXX XXXX XXXX
(15-12)	(11)	(10-0)

SRAM TEST: Set to 0 to indicate external data SRAM test passed OK.
                             Set to 1 to indicate external data SRAM failure.

X: Reserved bits

Note that the default external SRAM configuration is assumed to be 8K x 8.

After running the external SRAM test, the CT8020 device should be reset. This will re-initialize the external SRAM contents to their normal operational values. Running the SRAM test, destroys all the data values held in the external SRAM.

9.16.3 External Data SRAM Configuration

After reset, the default CT8020 configuration assumes an external byte-wide 8K x 8 data SRAM. The CT8020 can be configured to operate with an external 4K x 16 data SRAM. To set the SRAM configuration use the command:

Command   = 0801H   to select a 16-bit wide memory (25 ns)

Command   = 0821H   to select a 8-bit wide memory (25 ns)

This command does not generate a status response. When this command is received, it halts all current operations and performs an internal reset. After issuing this command, the host should wait for a period of 10 ms and then write the IDLE command (0000H) to the CT8020. Once this has been completed the Host should then re-configure the codec configuration before proceeding with further operations.

9.17 DEVICE IDENTIFICATION

9.17.1 Get Device Identification code

Command = 3400H

0011	01	00 0000 0000
(15-12)	(11-10)	(9-0)

Status

1000	0000	0010	0000
(15-12)	(11-8)	(8-4)	(3-0)

The status reply is the device code as a hexadecimal number i.e. CT8020 = 8020H.

9.17.2 Get Device Version (revision) code

Command = 3800H

0011	10	00 0000 0000
(15-12)	(11-10)	(9-0)

Status

XXXX	XXXX	XXXX	XXXX
(15-12)	(11-8)	(8-4)	(3-0)

XXXX = 4 bit hexadecimal code.

The status reply is the device version code as a hexadecimal number i.e. version 1.14 = 0114H.

9.18   TONE GENERATION in IDLE MODE

This command is used to generate tones in IDLE mode only. To generate DTMF tones during Standalone Speakerphone mode, please refer to the Speakerphone commands. When tone generation is completed, the Host should use the IDLE command to return the CT8020 to the IDLE state.

Generate Tone Command:

0110	000	MASTER GAIN	TONE INDEX
(15-12)	(11-9)	(8-5)	(4-0)

TONE INDEX: Selects the tone to be generated.

MASTER GAIN:

Modifies (reduces) the level of the tone to be generated with respect to the level programmed into the tone table. The level value in this field is added to the level value programmed into the tone table. The value resulting is used to select the output level (see table below). For example, if the tone table contains the level 5, and the master gain is set to level 8, the tone is actually output with level value of $5 + 8 = 13$. The result of the addition is limited $<= 15$, so if the tone level is 8, and the master gain is 9, the result $8+ 9 = 17$, is limited to 15 and the tone is output using level value 15. An alternate view of this control is note that the output level is reduced by MASTER GAIN x 2dB, with a minimum output level of -24 dB.

Status:

0110	0000 000	MASTER GAIN	TONE INDEX
(15-12)	(11-5)	(4)	(3-0)

With default output codec routing (= 00) tone is output via codec 0 only (telephone line side). To output tone to codec1, change the output codec routing in the codec configuration command.

Tone generation is possible in two mode: synchronous or asynchronous.

9.18.1   Synchronous mode

In this mode (default) the duration of the tone is determined by the number of frame periods for which the command is repeated. Synchronous mode is the default mode and is compatible with the tone generation of the CT8005 TrueSpeech Messaging Co-Processor.

The CT8020 creates the output waveform in frames of 30 ms each (240 samples at 8.0 KHz). The CT8020 will check for a host command at the end of each frame after updating the status response and asserting Status Ready in the Hardware Status Register. If the host repeats the original command, the status reply is repeated, and tone generation is continuous. If the host changes the tone parameters, the waveform output is changed accordingly. If the command is the IDLE command, tone generation is terminated. Note that the CT8020 requires that the IDLE command is used to correctly terminate tone generation. If the host does not issue any command, the CT8020 continues to check for a command every 30 ms and continues to generate the tone specified by the last command.

To generate a tone of 90 ms duration in this mode, the host performs the following sequence:

write tone command 60XXH
wait for Status Ready   (30 ms delay)
repeat tone command
wait for Status Ready   (30 ms delay)
repeat tone command
wait for Status Ready   (30 ms delay)
write idle command (0000H)
To generate a silence gap of 90 ms, use the above sequence with the tone command 6000H. This generates a special "silence" tone.

9.18.2 Asynchronous mode

In this mode, the on and off period for the tone, is pre-programmed by the host, and then complete generation of the tone (on and off periods) is executed with a single command. The host may poll the CT8020 during execution of the command to determine when generation of the complete tone has finished.

Additional Tone Mode Commands

SET SYNCHRONOUS (default, CT8005 compatible) TONE MODE

command: 6E00H
status: 6E00H

SET ASYNCHRONOUS TONE MODE

command: 6E01H
status: 6E01H

GET TONE MODE

command: 6E02H

if in synchronous mode
status: 0000H

if in asynchronous mode
status: 00001H

This command can be used to determine the current tone mode.

The following group of commands are only effective in ASYNCHRONOUS tone mode:

SET TONE ON PERIOD

command C1:   6E04H
status S1:   6E04H
command C2:   XXXXH = data value
status S2:   XXXXH = data value echoed

SET TONE OFF PERIOD

command C1:   6E05H
status S1:   6E05H
command C2:   XXXXH = data value
status S2:   XXXXH = data value echoed

GET TONE ON PERIOD

command: 6E06H
status: XXXXH = data value

GET TONE OFF PERIOD

command: 6E07H
status: XXXXH = data value

The units used for setting and reading the tone on and off period are 250 microseconds. By default the tone on and tone off periods are both set to 0192H (400 decimal) which is equivalent to a period of 100 ms, (i.e. 400 * 250 microseconds = 100 milliseconds).

GET TONE STATE

command: 6E03H

if tone generation is still in progress then
status: 0001H

otherwise
status: 0000H

9.18.3 Tone Generation in Asynchronous mode:

To generate a tone on = 90 ms followed by a tone off = 90 ms use the following sequence:

write SET ASYNCHRONOUS TONE mode command
wait for Status Ready in Hardware Status Register and read status response.
(this needs to be done only once)

write SET TONE ON PERIOD command
wait for Status Ready and read status response.
write tone on period value command = 0168H (0168H = 360 decimal, 360 * 250 us = 90 ms)
wait for Status Ready and read status response.
write SET TONE OFF PERIOD command
wait for Status Ready and read status response.
write tone off period value command = 0168H
wait for Status Ready and read status response.
(this needs to be done only once, unless the on/off period requires further change)

write tone command 60XXH
wait for Status Ready and read response

poll device using GET TONE STATE command
wait for Status Ready and check status reply to determine if tone has completed yet
(repeat this last step as often as required).

Once tone generation has been completed, the Host should issue the IDLE command.

9.18.4 Tone Level Table

Level Value (index)	Codec output level (dB relative to 0.707 Vrms)	Digital output level dBm0
0	+6	+1.5
1	+4	-0.5
2	+2	-2.5
3	0	-4.5
4	-2	-6.5
5	-4	-8.5
6	-6	-10.5
7	-8	-12.5
8	-10	-14.5
9	-12	-16.5
10	-14	-18.5
11	-16	-20.5
12	-18	-22.5
13	-20	-24.5
14	-22	-26.5
15	-24	-28.5

This table shows the actual tone output level as a function of the level value, calculated by adding the level value contained in the tone table to the level value specified in the MASTER GAIN field of the Generate Tone Command.

The codec output levels given are those produced by the VFR0 output pin of a Texas Instruments TP3054 mu-law codec when connected to the CT8020 (600 ohm load). Note that the TP3054 output is driven by a power amplifier with approximately 4 dB of gain. A digital signal at 0 dBm0 (0.775 Vrms) will produce an output signal of 1.3 Vrms (+4.5 dBm-600 ohms) at the codec output.

9.18.5 New Tone Initialization

Command (C1):

0110	10	00000	TONE INDEX
(15-12)	(11-10)	(9-5)	(4-0)

Status (S1):

0110	10	00000	TONE INDEX
(15-12)	(11-10)	(9-5)	(4-0)

Command (C2):

0110	0000	Gain 1	Gain 0
(15-12)	(11-8)	(7-4)	(3-0)

Status (S2):

0110	0000	Gain 1	Gain 0
(15-12)	(11-8)	(7-4)	(3-0)

Command (C3):

Frequency Factor for Tone 0
(15-0)

Status (S3)

Frequency Factor for Tone 0
(15-0)

Command (C4):

Frequency Factor for Tone 1
(15-0)

Status (S4)

Frequency Factor for Tone 1
(15-0)

TONE INDEX: index in range 1 to 31, index 0 is reserved for a "silent" tone.

Gain1,Gain0:   level value from tone level table

Frequency Factor: $32767 \times cosine(2 \times pi \times F/8000)$
where   pi = 3.14159
F is the desired frequency
8000 is the sample rate at which the codec is operating
Note : single frequencies can be generated by setting either frequency factor to
7FFFH

9.18.6 Default (Power-On) Tone Table Contents

Tone Index	Freq. 0	Gain 0	Freq. 1	Gain 1	DTMF Digit
0	No Tone				
1	697	1	1209	0	1
2	697	1	1336	0	2
3	697	1	1477	0	3
4	770	1	1209	0	4
5	770	1	1336	0	5
6	770	1	1477	0	6
7	852	1	1209	0	7
8	852	1	1336	0	8
9	852	1	1477	0	9
10	941	1	1209	0	* (Star)
11	941	1	1336	0	0
12	941	1	1477	0	# (Pound)
13	800	1			
14	1000	1			
15	1250	1			
16	950	1			
17	1100	1			
18	1400	1			
19	1500	1			
20	1600	1			
21	1800	1			
22	2100	1			
23	1300	1			
24	2450	1			
25	350	1	440	0	
26	440	1	480	0	
27	480	1	620	0	
28	697	1	1633	0	A
29	770	1	1633	0	B
30	852	1	1633	0	C
31	941	1	1633	0	D

Note that index zero is reserved for a silent tone. This can be used to generate gaps or pauses between tone, for example when generating a series of DTMF digits.

See Tone Level Table for gain value equivalent levels.

9.19 CT8020 Line Monitor Commands

(firmware revision 0112 or higher only)

The CT8020 Line Monitor command can be used to access 5 detectors (1 DTMF and 4 Call Progress). These detectors can be individually enabled or disabled. When enabled, the detectors run whenever the CT8020 is in any of the following modes: Line Monitor, Record, Playback or Full-Duplex Speech (record+playback) mode. By default all the detectors are disabled.

9.19.1 Line Monitor Command

Command (7000H)

0111	0000	0000	0000
(15-12)	(11-8)	(7-4)	(3-0)

Synchronous Mode Status:

0111	F3	F2	F2	F0	0	PEAK	DTMF VALID	CPF VALID	DTMF DIGIT
(15-12)	(11)	(10)	(9)	(8)	(7)	(6)	(5)	(4)	(3-0)

Asynchronous Mode Status

ls 4-bits Frame Count	F3	F2	F2	F0	0	PEAK	DTMF VALID	CPF VALID	DTMF DIGIT
(15-12)	(11)	(10)	(9)	(8)	(7)	(6)	(5)	(4)	(3-0)

This command activates Line Monitor Mode. To terminate Line Monitor Mode use the IDLE command (0000H). If asynchronous mode is selected (see below) it can also be used during record/playback to poll the state of the detectors.

DTMF DIGIT	The DTMF digit value (only valid if DTMF VALID is set) : 1-9 1-9 0 0BH * 0AH # 0CH A 0DH B 0EH C 0FH D 0
CPF VALID	Indicates that at least 1 of the 4 detector outputs F0-F3 is set (logical OR of F0-F3)
DTMF VALID	Set when a valid DTMF digit is detected
PEAK	Only valid when RECORD is active. This bit has the same meaning as the PEAK bit in the Record S2 status response
F0-F3	Individual filter output valid bits for filters 0 -3
ls 4-bits Frame Count	Only present when asynchronous mode is selected. This field can be used by the host to track the number of frames processed by the CT8020 since the last Line Monitor Status.

9.19.2 Synchronous and Asynchronous Monitor Mode

By default the Line Monitor Command operates in synchronous mode (CT8005 compatible). In this mode the Line Monitor Status response is delayed until completion of processing of the next 30 ms frame. In this mode the Line Monitor Status response can be used as a "frame clock" since the status response is synchronized to the frame period. For continuous monitoring the Host should issue a new Line Monitor Command each frame period (each time the previous Line Monitor Status response is received). Note that in Synchronous Mode, after issuing the Line Monitor command, the Host must wait for the (delayed) status response before it can issue another command.

In Asynchronous Mode, the status response to the Line Monitor Command is immediate. The status reported represents the most recent 30 ms frame processed. To assist the Host in correlating the time of the response with other system events, the ms 4-bits of the response contain the ls 4-bits of the CT8020's internal frame counter. This frame counter increments once every 30 ms frame period. This count value can be used by the Host to measure the duration of a valid filter output.

Asynchronous mode should be selected if the Host needs to poll the detectors during record/playback.

to select Synchronous mode, use the command:

Set Synchronous Mode   7E00H
Status Response   7E00H

to select Asynchronous mode, use the command:

Set Asynchronous Mode   7E01H
Status Response   7E01H

to read the current mode, use the command:

Read Sync Mode   7E02H
Status Response   0000H = Synchronous Mode
                              0001H = Asynchronous Mode

9.19.3 Enabling and Disabling the DTMF Detector

To Enable the DTMF Detector, use the command

Enable DTMF Detector   5151H
Status Response   5151H

To Disable the DTMF Detector, use the command

Disable DTMF Detector   5150H
Status Response   5150H

9.19.4 Controlling the Call Progress Tone Filters F0-F3

The CT8020 includes 4 Call Progress Filters. Each filter can be addressed using the select filter command to set the current value of the CT8020's filter ID parameter (CPFID):

Select Filter Command (5154H - 5157H)

0101	0001	0101	01	SELECT
(15-12)	(11-8)	(7-4)	(3-2)	(1-0)

Status Response (5154H - 5157H)

0101	0001	0101	01	SELECT
(15-12)	(11-8)	(7-4)	(3-2)	(1-0)

SELECT = CPFID
00   Filter F0
01   Filter F1
10   Filter F2
11   Filter F3

Once Selected, the following commands can be used to control the filter:

Filter Enable (5153H)
Filter Disable (5152H)

Status response:

0000	000	DTMF Detector Enabled	0000	F3	F2	F1	F0
(15-12)	(11-9)	(8)	(7-4)	(3)	(2)	(1)	(0)

The F3-F0 and DTMF Detector Enabled bits are set to show which filters are enabled.

To enable all 4 filters the following command sequence can be used

Command	Status Response	Action
5154H	5154H	Select Filter F0
5153H	0001H	Filter F0 is enabled
5155H	5155H	Select Filter F1
5153H	0003H	Filters F1+F0 are enabled
5156H	5156H	Select Filter F2
5153H	0007H	Filters F2+F1+F0 are enabled
5157H	5157H	Select Filter F3
5153H	000FH	Filters F3+F2+F1+F0 are enabled

9.19.5 Reading the Filter Energy Output

The actual Filter Energy output values can be read using the following command (516XH):

0101	0001	0110	FILTER	INDEX
(15-12)	(11-8)	(7-4)	(3-2)	(1-0)

FILTER
00	F0
01	F1
10	F2
11	F3

INDEX
00	Broadband Energy ls word (bits 15-0)
01	Broadband Energy ms word (bits 31-16)
10	In Band Energy ls word (bits 15-0)
11	In Band Energy ms word (bits 31-16)

The status response contains the 16-bit value selected by INDEX.

Each filter provides two 32-bit energy parameters:
The broadband energy of the un-filtered input signal.
The in-band energy at the filter output.

The energy value is calculated over a 240 sample (30 ms) input frame:

$$\text{Energy} = 1/32 \ * \ \sum \ (x/4) * (x/4)$$

If more than one filter is enabled, the broadband energy from each enabled filter will be the same.

9.19.6 Selecting the Filter Characteristics

The CT8020 includes Filter Parameters Sets for 8 different call progress tone (CPT) fixed filters plus an additional set of 4 Filter Parameters that may be programmed by the host. Each of the four filters F0-F1 can be mapped onto any of the 12 available filter parameter sets. The first 4 filter parameter sets are stored in the CT8020s internal RAM and may be re-programmed by the host.

Filters   Mapping Table   Filter Set

Filter F0	2
Filter F1	10
Filter F2	9
Filter F3	11

Programmable Set 0
Programmable Set 1
Programmable Set 2
Programmable Set 3

Fixed Set 4
Fixed Set 5
Fixed Set 6
Fixed Set 7
Fixed Set 8
Fixed Set 9
Fixed Set 10
Fixed Set 11
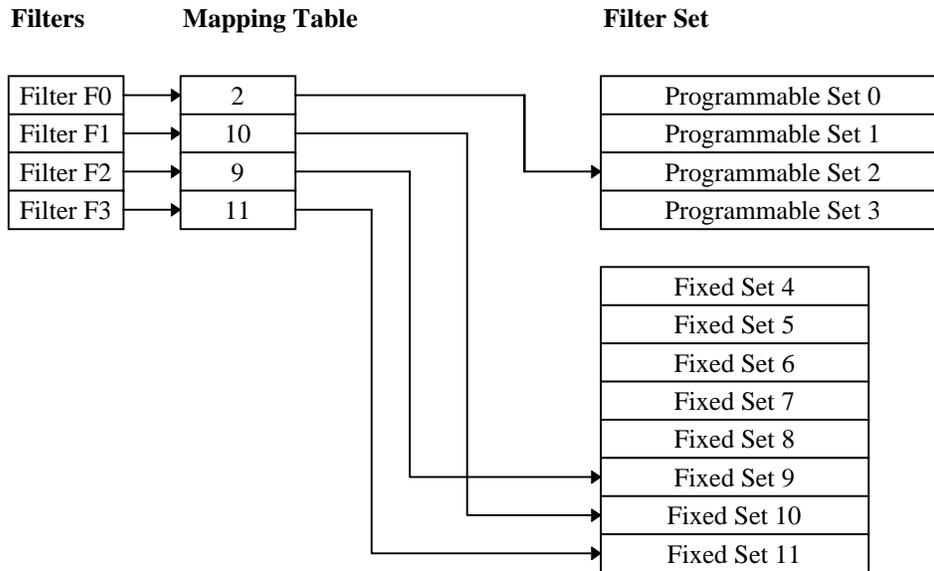
Figure 9-4 Filter Mapping

The following table shows the default contents of the Filter Parameter Sets

Filter Parameter Set	
0	Programmable Filter Set 0 (by default this is loaded with Fixed Set 4)
1	Programmable Filter Set 1 (by default this is loaded with Fixed Set 5)
2	Programmable Filter Set 2 (by default this is loaded with Fixed Set 6)
3	Programmable Filter Set 3 (by default this is loaded with Fixed Set 7)
4	Fixed Filter Set 4 (wide CPT filter 300Hz - 640 Hz)
5	Fixed Filter Set 5 (narrow CPT filter 300Hz - 500 Hz)
6	Fixed Filter Set 6 (fax calling tone CNG 1100Hz +/- 5%)
7	Fixed Filter Set 7 (350 Hz +/- 5%)
8	Fixed Filter Set 8 (400 Hz +/- 5%)
9	Fixed Filter Set 9 (480 Hz +/- 5%)
10	Fixed Filter Set 10 (440 Hz +/- 5%)
11	Fixed Filter Set 11 (620 Hz +/- 5%)

The Filter Parameter Set used by each of the Filters F0-F3 may be programmed by the Host. The filter set used by each filter is controlled by the CT8020's Filter Parameter Set Mapping Table. The default Filter Set selection is shown below:

Default Filter Parameter Set Mapping Table

FILTER	Table Value	Filter Parameter Set used by Filter
F0	0	Programmable Filter Set 0 (equivalent to Fixed Set 4 after reset)
F1	1	Programmable Filter Set 1 (equivalent to Fixed Set 5 after reset)
F2	2	Programmable Filter Set 2 (equivalent to Fixed Set 6 after reset)
F3	3	Programmable Filter Set 3 (equivalent to Fixed Set 7 after reset)

So after reset the following filter parameters are selected

FILTER	Filter Parameter Set used by Filter
F0	wide CPT filter 300Hz - 640 Hz
F1	narrow CPT filter 300 Hz - 500 Hz
F2	fax calling tone CNG filter 1100 Hz +/- 5%
F3	350 Hz +/- 5%

At reset, the filter parameters in Programmable Filter Sets 0-3 are loaded from the parameters in Fixed Filter Sets 4-7.

After reset, the Programmable Filter Sets may be re-loaded from Fixed Filter Sets using the following command:

Restore Initial Filter Parameters Command   515DH
Status Response   515DH

9.19.7 Changing the Filter Parameter Set Mapping Table

The contents of the Filter Parameter Set Mapping Table can be changed using the following:

Command (517XH):

0101	0001	0111	MAPPING VALUE
(15-12)	(11-8)	(7-4)	(3-0)

Status Response:

0101	0001	0111	MAPPING VALUE
(15-12)	(11-8)	(7-4)	(3-0)

Where MAPPING VALUE is in the range 0-11 (decimal) corresponding to Filter Parameter Sets 0-11.

To change a Filter Parameter Set Mapping Table entry:

1. First select the entry to be changed (F0-F3) using the Select Filter Command 5144H-5147H
2. Change the table entry using the command 517XH.

The following Mapping Table can be created using the command sequence below:

FILTER	Table Value	Filter Parameter Set used by Filter
F0	7	Set 7 = 350 Hz
F1	10	Set 9 = 440 Hz
F2	9	Set 10 = 480 Hz
F3	11	Set 11 = 620 Hz

Command Sequence:

5154H	Select Filter F0
5177H	Select Filter Set 7
5155H	Select Filter F1
517AH	Select Filter Set 10
5156H	Select Filter F2
5179H	Select Filter Set 9
5157H	Select Filter F3
517BH	Select Filter Set 11

9.19.8 Filter Detection Algorithm

The Filter Detection Algorithm has three stages:

1. The In-Band filter energy for each 15 ms half-frame (120 samples) is compared against a minimum threshold. By default, this is set to approximately -37 dBm0. If the energy is less than the threshold a "no detect" decision is made for the half-frame.
2. The In-Band filter energy for each 15 ms half-frame (120 samples) is compared against the Broad-Band energy. If the In-Band energy is greater than 21/32 * Broad-Band energy then a "detect" decision is made for the half-frame.
3. A filter detect history is constructed every frame period which covers the last 4 frames, or 8 half-frames. If a detect decision was made in at least 5 of the last 8 half-frames, then the corresponding Filter Output Valid bit is set in the Line Monitor Status response.

Note: dBm0 scale - For a mu-law or a-law codec, the full scale input signal range of the codec corresponds to approximately 3.14 dBm (0 dBm is 1 mW in 600 ohms). For signal level compatibility across digital systems this signal level is referred to as 3.14 dBm0. When using a 16-bit linear codec, the full scale range of this codec is also assumed to be 3.14 dBm0.

9.19.9 Reading the Filter History Register

The Filter History Register for each Filter F0-F3 can be read using the command:

Command (515CH)

0101	0001	0101	1100
(15-12)	(11-8)	(7-4)	(3-0)

Status:

....	n-12	n-11	n-10	n-9	n-8	n-7	n-6	n-5	n-4	n-3	n-2	n-1	n
(15-13)	(12)	(11)	(10)	(9)	(8)	(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)

The status response shows the detection decision for the most recent 15 ms half-frame "n" and up to the last 15 half-frames "n-1" to "n-15". By default, the CT8020 only checks from n to n-7, with n-8 to n-15 ignored. The default detection algorithm looks for five "1" bits in the range "n" to "n-7".

To read the History Register for Filter F1, use the following command sequence:

Command	Status Response	Action
5155H	5155H	Select Filter F1
515CH	XXXXH	Filter F1 History Register is read

9.19.10 Reading the Frame Counter

The CT8020's internal 16-bit frame counter can be read using the command

Command (5144H):

0101	0001	0100	0100
(15-12)	(11-8)	(7-4)	(3-0)

Status:

16-bit Frame Counter
(15-0)

9.19.11 Programming the CT8020 Filters

Filter Parameter Sets 0-3 can be programmed by the Host. The Filter Parameter Set to be programmed is selected by the CPFID parameter set using the Filter Select command 5154H-5157H.

Each Filter Parameter Set contains 19 words of parameter data.

To start programming of the Filter Parameter Set, use the command:

Command (**515BH**):

0101	0001	0101	**1011**
(15-12)	(11-8)	(7-4)	(3-0)

Status (515EH)

0101	0001	0101	**1011**
(15-12)	(11-8)	(7-4)	(3-0)

After writing this command, the next **19** words written to the Software Control Register (command register) will be written to the Filter Set selected.

Command (XXXXH):

Filter Parameter Set Data Word
(15-0)

Status (XXXXH):

Filter Parameter Set Data Word
(15-0)

Note that the earlier **CT8020A11BQC** (firmware revision 0112) only allowed downloading of the first **15** words of the filter parameter set. This was implemented using the **515EH** command. The new **515BH** command implemented in the **CT8020D11AQC** (firmware revision 0114) allows downloading of all **19** parameters in the filter parameter set. The CT8020D11AQC continues to support the **515EH** command for purposes of backwards compatibility with the older CT8020 version.

The filter data consists of 15 words of filter coefficients for the sixth order filter (3 x 5 words), plus 4 additional control parameters.

Each filter is a sixth order filter constructed from 3 cascaded second order stages.

The following shows the parameter order and example values for Fixed Filter Set 4 (300-640 Hz) :

Word	Example Value	Description
0	28967	A1 (Q14) = 1.768028
1	-28798	A2 (Q15) = -0.878854
2	-1988	B2 (Q15) = -0.060682
3	0	B1 (Q14) = 0
4	1988	B0 (Q15) = 0.060682
5	28017	A1 (Q14) = 1.710051
6	-30963	A2 (Q15) = -0.944905
7	12605	B2 (Q15) = 0.384666
8	0	B1 (Q14) = -0.620271
9	12607	B0 (Q15) = 0.384720
10	31398	A1 (Q14) = 1.916387
11	-31859	A2 (Q15) = -0.972276
12	30541	B2 (Q15) = 0.932033
13	-30020	B1 (Q14) = -1.832294
14	30542	B0 (Q15) = 0.932074
15	7	Internal Filter numeric scaling
16	159	Minimum in-band energy threshold
17	21	21/32 in-band to broad-band ratio parameter
18	0FF5H	shift-mask = 0FFH, bit count=5 for History test

Q15 format uses 32768 to represent 1.000
Q14 format uses 16384 to represent 1.000

The Internal filter numeric scaling is set to compensate for the internal gain within the filter in order to prevent numeric overflow. The higher the internal gain (Q factor), the lower the numeric scaling value required. For a narrow band pass filter (high Q)this should be set to around 5, for a wide band pass filter this should be set to around 7. The value used is best determined by experimentation, by looking for non linearity in the filter output value as a function of input signal frequency and level.

The Minimum in-band energy is squared by the CT8020 and used to compare against the in-band filter energy.

The in-band to broad-band ratio parameter is used to create a scaling ratio by dividing by 32 and using the resulting fractional multiplier to scale the broad-band energy for comparison with the in-band energy.

The final parameter is split into two parts. The ms 12-bits create an AND mask to control how many History Register bits are counted. The ls 4 bits provide the bit count threshold 0-15 for counting the "1" bits in the History Register.

The filter coefficients themselves have to be created using special Digital Filter Design Software. This software is available from a number of sources specializing in DSP design software. Filter design packages vary in the nomenclature used to label the A and B parameters as well the sign value +/- of the constants. The best approach to take when designing a new filter, is to first create a design for the 300-640 Hz filter defined above. The filter coefficients generated can usually be approximately compared against the example above to determine if any of the parameters need to be re-ordered or have their sign +/- inverted.

The example filter above (300-640 Hz) was designed with the following parameters:

type	6th order elliptic
lower stop-band cut-off	250 Hz
lower pass-band cut-off	300 Hz
upper pass-band cut-off	640 Hz
upper stop-band cut-off	800 Hz
sample rate	8000 Hz
pass band ripple	0.1 (1 dB)
stop band ripple	0.05 (-26 dB stop band attenuation)

9.20 STANDALONE SPEAKERPHONE

9.20.1 Enter Standalone Speakerphone Mode Command:

This command is not available in DSVD Speakerphone mode.

1110	01	01	Line Sensitivity	Microphone Sensitivity	Priority	0
(15-12)	(11-10)	(9-8)	(7-5)	(4-2)	(1)	(0)

Status:

1110	01	01	Line Sensitivity	Microphone Sensitivity	Priority	0
(15-12)	(11-10)	(9-8)	(7-5)	(4-2)	(1)	(0)

Line Sensitivity:

000	2 dB
001	4 dB
010	6 dB
011	8 dB (normal setting)
100	10 dB
101	12 dB
110	14 dB
111	16 dB

Microphone Sensitivity:

000	2 dB
001	4 dB
010	6 dB (normal setting)
011	8 dB
100	10 dB
101	12 dB
110	14 dB
111	16 dB

The line and microphone sensitivity determine the signal-to-noise ratio (SNR) at which the voice detectors for the transmit and receive directions will be activated. The voice detectors are used in half-duplex mode to determine which direction is talking, and which direction should be attenuated.

Priority:

0	both directions have equal priority
1	microphone side (near end) has priority

The priority control is used to determine the behavior of the system when both directions are silent. In the equal priority (or no priority) mode, the loop attenuation is distributed equally between the receive and transmit directions. If the priority bit is set, the line side is given all the attenuation and the microphone (near end) as priority.

Before entering Standalone Speakerphone mode, the Codec Configuration must be programmed with Output Codec set to 00 and Input Codec set to 0.

9.20.2 Get Speakerphone Status Command:

This command may be used in DSVD Speakerphone mode.

1110	000	0 0000 0000
(15-12)	(11-9)	(8-0)

Status:

1110	000	0	Direction	0	Current Loop Attenuation
(15-12)	(11-9)	(8)	(7-4)	(3)	(2-0)

Current Loop Attenuation: This indicates the amount of loop attenuation currently in use.
See Set Speakerphone Parameters command below for the format of this field.

Direction: This indicates which direction (microphone/speaker) is considered active by the CT8020 Speakerphone control logic. This is a 4 bit field used to represent the number range from +7 to -8. The most positive values indicated that the signal from the microphone side is dominant (microphone speaking). The most negative values indicate that the signal from the line side is dominant (telephone line speaking). Values in the center of the range can either indicate a transition from one side to the other, or if the value stays at approximately the zero position, indicates that neither side is talking.

+7	0111	
+6	0110	Microphone side is speaking.
+5	0101	
+4	0100	
+3	0011	Transition to/from microphone active
+2	0010	
+1	0001	
0	0000	Both sides silent (constant energy) or transition
-1	1111	
-2	1110	
-3	1101	
-4	1100	Transition to/from line side active
-5	1011	
-6	1010	
-7	1001	Line side is speaking
-8	1000	

9.20.3 Set Speakerphone Parameters Command:

This command may be used in DSVD Speakerphone Mode

1110	001	Line Volume	Speaker Volume	Loop Attenuation
(15-12)	(11-9)	(8-7)	(6-3)	(2-0)

Status:

1110	001	Line Volume	Speaker Volume	Loop Attenuation
(15-12)	(11-9)	(8-7)	(6-3)	(2-0)

Line Volume: This controls the volume transmitted to the telephone line

00   +8 dB
01   +4 dB
10   +0 dB (normal setting)
11   Mute Microphone

Speaker Volume: This controls the volume to the speakerphone loudspeaker.

0000   +14 dB
0001   +12 dB
0010   +10 dB
0011   +8 dB
0100   +6 dB
0101   +4 dB
0110   +2 dB
0111   0 dB (normal setting)
1000   -2 dB
1001   -4 dB
1010   -6 dB
1011   -8 dB
1100   -10 dB
1101   -12 dB
1110   -14 dB
1111   Speaker Mute

Loop Attenuation : Total attenuation used by receive and transmit attenuators

Full Duplex Operation
000   0 dB
001   -4 dB
010   -8 dB
Half Duplex Operation
011   -12 dB
100   -16 dB (startup condition)
101   -20 dB
Abnormal Conditions
110   -24 dB
111   -28 dB

9.20.4 SpeakerPhone Configuration Command:

This command may be used in DSVD Speakerphone mode provided that Line Training = 00.

1110	010	0 0000	Line Training	Automatic Loop Adjustment
(15-12)	(11-9)	(8-4)	(3-2)	(1-0)

Status:

1110	010	0 0000	Line Training	Automatic Loop Adjustment
(15-12)	(11-9)	(8-4)	(3-2)	(1-0)

Automatic Loop Adjustment:

00:	Loop Attenuation is not automatically adjusted
01:	Increase loop attenuation by 12 dB on detection of abnormal conditions. Maintain modified attenuation until a new command is received from host.
10:	Increase loop attenuation by 12 dB on detection of abnormal conditions. Attempt to restore normal loop attenuation when possible. This is the preferred (normal) setting.
11:	Reserved

Line Training:

00:	Do not modify line-side (electrical) echo canceller settings.
01:	Send training pulse to line to set (electrical) echo canceller coefficients.
10:	Reserved
11:	Reserved

When the Acoustic Echo Canceller (AEC) is active in DSVD speakerphone mode, the Line Training field should always be set to 00.

9.20.5 Generate Tone (in speakerphone mode):

This command is not available in DSVD Speakerphone mode.

1110	100	Master Gain	Tone Index
(15-12)	(11-9)	(8-5)	(4-0)

Status

1110	100	Master Gain	Tone Index
(15-12)	(11-9)	(8-5)	(4-0)

See Generate Tone command (mode 6) for usage.
Each command/status interaction generates tone for 30 ms.
This command is not available in DSVD speakerphone mode.

Use Tone Index #0 to generate silence between dialed digits. During tone generation, the speech path
between codec 0 and codec 1 is disabled. To re-enable this path at the end of DTMF dialing, the host
should issue command E000H (Get SpeakerPhone Status). This is used to inform the CT8020 that dialing is
complete.

9.20.6 Get Electrical Echo Canceller Quality Factor Command:

This command is not available in DSVD Speakerphone mode.

1110	101	0 0000 000	HIWORD
(15-12)	(11-9)	(8-1)	(0)

Status:

Electrical Echo Canceller Quality Factor

This command returns either the low (HIWORD = 0) order or high order (HIWORD = 1) 16 bits of the
electrical (line-side) echo canceled 32-bit quality factor. The quality factor is a measure of how well the
training pulse succeeded in configuring the electrical echo canceller coefficients.

During training, the echo canceller sends the training pulse and receives an echo of the training pulse back
from the line. The echo canceller coefficients are adjusted to achieve maximum cancellation of the training
pulse echo.

If no echo occurs (for example, if a 4-wire telephone connection is used), all the echo canceller coefficients
are set to zero, no cancellation is required ("perfect" cancellation is achieved - there is no reflected signal),
and the quality factor is zero in all 32 bits.

If the training pulse is sent while there is a high level incoming signal (dial tone for example), the echo
canceller is unable to cancel the incoming signal (training pulse echo + dial tone) and the quality factor
becomes very large (> 100000H). This indicates that training failed and that full duplex operation of the
speakerphone can not be activated (loop attenuation must be greater than or equal to 12 dB).

If the training pulse echo is successfully canceled, the quality factor should be less than 10000H (all high order bits zero). Under these circumstances, full duplex speakerphone operation may be selected (loop attenuation less than 12 dB).

If the training pulse has not been sent, the quality factor will be set to FFFFFFFFH.

The numbers given here are approximate, and depend to a great extent on the design of the external hardware. The user is expected to experiment and discover suitable threshold values appropriate to the users hardware environment.

Note that this command reports the current value of the Electrical Echo Canceller (EEC) Quality Factor. Since training of the EEC takes several milliseconds, it is possible to read this value before training has completed. In this case the Quality Factor from the state prior to training will be read. The host should allow around 50 ms to elapse between sending the command to train the EEC and attempting to read the new Quality Factor. During the training period, the host should not issue any additional commands to the CT8020, as this will delay or disrupt the training process.

See Appendix A for additional information.

9.21 HOST-TO-HOST DATA COMPRESSION AND DECOMPRESSION

The CT8020 can be operated as a full or half-duplex TrueSpeech compression engine in a codec-less configuration. In this situation, the CT8020 routes the uncompressed data stream to the host instead of to the codec.
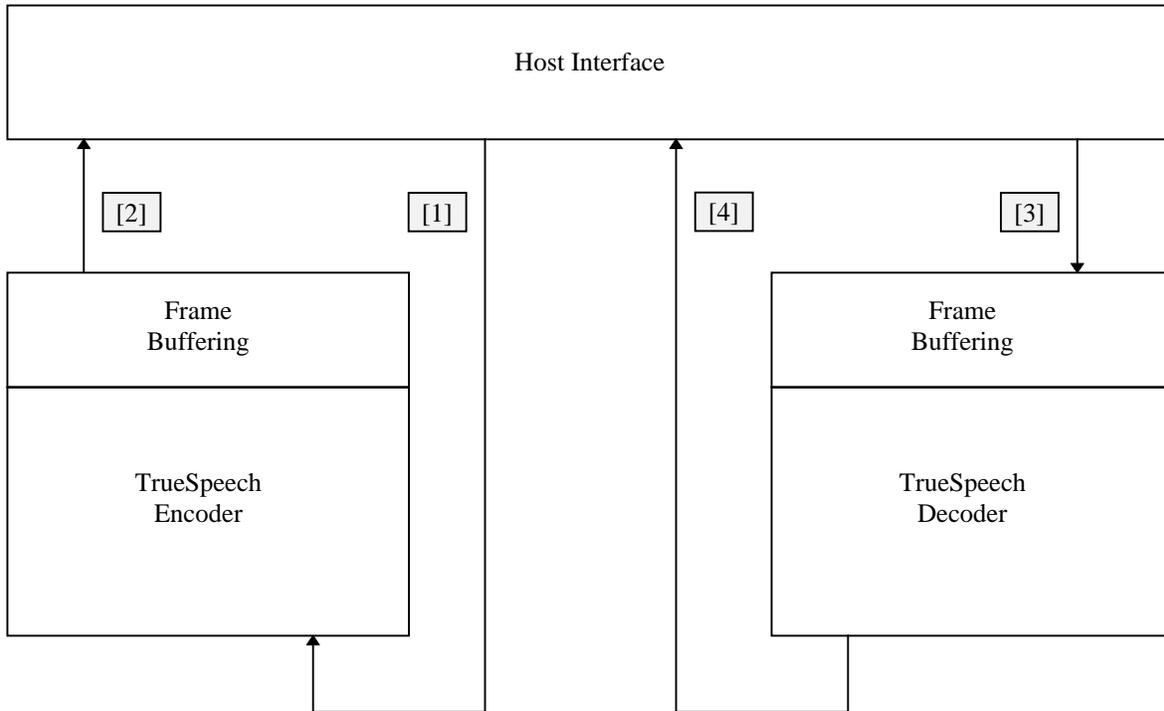
Figure 9-5 Host-to-Host Operation

The Host-to-Host compression/decompression protocol is structured so that the four data exchange operations are independent. The four data exchange operations that take place are:

1. Un-compressed 16-bit linear data transfer from host to CT8020, denoted using [1] in the description below.
2. Compressed TrueSpeech data transfer from CT8020 to host, denoted using [2] in the description below.
3. Compressed TrueSpeech data transfer from host to CT8020, denoted using [3] in the description below.
4. Un-Compressed 16-bit linear data transfer from CT8020 to host, denoted using [4] in the description below.

The compressed data exchanges, [2] and [3] to and from the CT8020 internal Frame Buffers take place using the same transfer protocol as used for record and playback (TFR Mode = 00). The Host should ensure that the AEC (Acoustic Echo Canceller) state is set to OFF for Host-to-Host operation.

9.21.1 Host-to-Host compression

Host-to-Host compression from the Host viewpoint is similar to the record process. The protocol used to transfer compressed data frames from the CT8020 to the host [2] is the same as that used for recording in DATA sync mode with TFR Mode = 00. However, instead of using the Record C1 command to start the process, the Host-to-Host compression C1 command is used. The compression C1 command is also used to transfer the actual uncompressed data frames to the CT8020 [1].

The following command is used to start Host-to-Host compression:

Compress Command C1 (= FXXXH):

1111 01	RECMODE	000 0	TFR_MODE	DATA
(15-10)	(9-7)	(6-3)	(2-1)	(0)

Status Response S1:

1111 01	RECMODE	000 0	TFR_MODE	READY
(15-10)	(9-7)	(6-3)	(2-1)	(0)

9.21.1.1 Recording (Compression) Modes

RECMODE	Recording Modes
000	TrueSpeech at 8.5, 6.3, 5.3, 4.8 or 4.1 Kbits/sec
001	Reserved
010	Reserved
011	Reserved
100	64 Kbit/sec A-law / Mu-law PCM (120 words per 30ms data frame)
101	128 Kbit/sec 16-bit linear (240 words per 30ms data frame)
110	64 Kbits/sec 8-bit signed linear (120 words per 30 ms data frame)
111	64 Kbits/sec WSS 8-bit unsigned linear (120 words per 30 ms data frame)

See Record section for more details on RECMODE and TFR_MODE.

DATA

In the first C1 command (used to start compression) the DATA flag is set by the host to indicate whether the host wishes to immediately transfer the first un-compressed speech frame [1] to the CT8020 for compression.

In subsequent compression C1 commands, the DATA flag is ignored by the CT8020. In this case the CT8020 always assumes that the host will be ready to transfer uncompressed data [1].

READY

If the READY flag is set in the status response, the CT8020 expects that immediately following the S1 response, the host will transfer 240 words (480 bytes) of uncompressed data. The READY flag will always be set in the first S1 response if the host set the DATA flag in the first C1 command. When the Host receives a status response with the READY flag set, it MUST immediately commence the transfer of uncompressed speech data.

Host-to-Host compression data transfer [1] and [2]

Host starts compression process [1] by issuing compression C1 command, and waits for Status Ready in the Hardware Status Register to be asserted.
CT8020 acknowledges start of compression with compression S1 response.
IF the READY flag is set in status response S1:

> Host transfers uncompressed data by writing the (240) uncompressed data words to the Software Control register and waiting for STATUS READY to be set after each word written. Each time STATUS READY is set, the host must read the Software Status Register in order to clear STATUS READY. The actual value read from the Software Status Register is the same as (echo of) the last data word written.

The compression C1, and S1 status response - READY flag are used to control subsequent un-compressed speech data transfers[1] to the CT8020.

Once compression has been started, the Host transfers compressed data from the CT8020 [2] using the normal record data transfer protocol (TFR Mode = 00 or 11).

The record protocol used to transfer compressed speech data frames from the CT8020 also supports the BUFFER MONITORING, FRAME CREATE, FRAME DELETE, and RECORD STOP commands.

Host-to-Host compression can be terminated either using the RECORD STOP command or the IDLE command. One of these commands should be issued during the command-status sequence in place of the compression C1 command.

Compression READY polling

Instead of using the compression S1 status READY response to determine if the CT8020 is ready to accept more uncompressed speech data, the Host can poll the READY state using the following command:

command: 5119H
status: 0000H   if CT8020 is ready to accept more uncompressed data.
                        0001H   if CT8020 is NOT ready to accept more uncompressed data.

This command is only valid if compression mode is active.

The advantage this command offers over simple use of the compression C1-S1 command-status, is that it allows the host to query the READY state without immediately committing to performing the data transfer. With the compression C1-S1 command-status, if the READY bit in the S1 status response is set, the host MUST immediately transfer data.

9.21.2 Host-to-Host decompression

Host-to-Host decompression is from the Host viewpoint is similar to the playback process. The protocol used to transfer compressed data frames from the Host to the CT8020 [3] is the same as that used for playback in DATA sync mode. However, instead of using the Playback C1 command to start the process, the Host-to-Host decompression C1 command is used. Note that in the case of decompression, the host must still send the playback C2 and C3 commands after sending the decompression C1 command to start the decompression process. The decompression C1 command replaces the playback C1 command, but the playback C2 and C3 commands are still required when starting decompression. The decompression C1 command is also used to transfer the actual uncompressed data frames from the CT8020 [1].

The following command is used to start Host-to-Host decompression:

Decompress Command C1:

1111 11	PLAYMODE	000 0	TFR_MODE	0
(15-10)	(9-7)	(6-3)	(2-1)	(0)

Status Response S1:

1111 11	PLAYMODE	000 0	TFR_MODE	READY
(15-10)	(9-7)	(6-3)	(2-1)	(0)

When starting decompression this command must then be followed immediately by the playback C2 and C3 commands. Note that when the first decompression C1 command is sent to start decompression, the READY flag in the status response will not be set, since at this point the CT8020 will have no decompressed data available.

To Start Playback: To Start Decompression:

Playback C1   Decompress C1
Playback C2   Playback C2
Playback C3   Playback C3

9.21.2.1 Playback (Decompression) Modes

PLAYMODE	Playback Modes
000	TrueSpeech at 8.5, 6.3, 5.3, 4.8, 4.1 Kbits/sec
001	Reserved
010	64 Kbit/sec A-law / Mu-law PCM (120 words per 30ms data frame)
011	Reserved
100	64 Kbits/sec 8-bit signed linear (120 words per 30 ms data frame)
101	64 Kbits/sec 8-bit unsigned linear (120 words per 30 ms data frame)
110	128 Kbits/sec 16-bit signed linear (240 words per 30 ms data frame)
111	Reserved

See Playback Mode section for more details on PLAYMODE and TFR_MODE.

READY

If the READY flag is set in the status response, the CT8020 expects that immediately following the S1 response, the host will transfer 240 words (480 bytes) of uncompressed data. When the Host receives a status response with the READY flag set, it MUST immediately commence the transfer of uncompressed speech data.

Host-to-Host decompression data transfer [3] and [4]

Host starts decompression process [3] by issuing decompression C1 command, and waits for Status Ready bit in the Hardware Status Register to be asserted.
CT8020 acknowledges start of decompression with decompression S1 response.
Host reads S1 status, Status Ready is cleared.
(Since no data has been decompressed at this time the READY flag will not be set)
Host sends playback C2 and C3 commands

Once decompression has been started, the Host transfers compressed data to the CT8020 [3] using the normal playback data transfer protocol.

Subsequent de-compressed speech is transferred using the decompression C1 command. The S1 status - READY flag is used to control the transfers :

Host sends decompression C1 command
CT8020 returns S1 status response including READY flag.
IF the READY flag is set:
    Host transfers de-compressed data by writing the dummy de-compression command F000H to the Software Control register and then waiting for STATUS READY to be set. Each time STATUS READY is set, the host must read the Software Status Register in order to clear STATUS READY. The data read from the Software Status Register is the de-compressed data. The host writes the F000H command 240 times in order to read 240 data words from the Software Status Register.

The playback protocol used to transfer compressed speech data frames to the CT8020 also supports the BUFFER MONITORING, FRAME CREATE, FRAME DELETE, and PLAYBACK STOP commands.

Host-to-Host decompression can be terminated either using the PLAYBACK STOP command or the IDLE command. One of these commands should be issued during the command-status sequence in place of the playback C2 command.

Decompression READY polling

Instead of using the decompression S1 status READY response to determine if the CT8020 is ready with more uncompressed speech data, the Host can poll the READY state using the following command:

command: 5219H
status: 0000H   if CT8020 is ready to provide more uncompressed data.
                0001H   if CT8020 is NOT ready to provide more uncompressed data.

This command is only valid if decompression mode is active.

The advantage this command offers over simple use of the decompression C1-S1 command-status, is that it allows the host to query the READY state without immediately committing to performing the data transfer. With the decompression C1-S1 command-status, if the READY bit in the S1 status response is set, the host MUST immediately transfer data.

9.21.3 Full Duplex Host-to-Host Compression-Decompression

The following command sequence is recommended for performing full duplex Host-to-Host Compression-Decompression. The sequence is described in summary form, for details on the individual steps listed, see the detailed descriptions above.

Start decompression using the decompression C1 command and playback C2 and C3 commands.
Start compression using the C1 command with DATA set to zero.

Perform data transfers using the following command loop:

> Check if CT8020 is ready for more playback data using the playback BUFFER MONITORING command.
> If the playback buffer is empty:
>> Transfer compressed speech data to CT8020.

> Check if the CT8020 has decompressed data ready using the decompression READY polling command.
> If the CT8020 has decompressed data ready (status = 0000H):
>> Transfer uncompressed speech data from CT8020.

> Check if the CT8020 is ready to accept data for compression using the compression READY polling command.
> If the CT8020 is ready to accept more data for compression (status = 0000H):
>> Transfer uncompressed speech data to CT8020.

> Check if the CT8020 has record data available using the record BUFFER MONITORING command.
> If the record buffer is not empty:
>> Transfer compressed speech data from CT8020.

Repeat the above loop until all data has been processed.

Terminate the process after reading the last uncompressed playback data and reading the last compressed record data from the CT8020 by issuing the IDLE command

9.22 TEST MODES

The CT8020 includes test modes which are useful in verifying device and system operation.

9.22.1 Test Mode 1: count mode

Command: 511FH
Status: 511FH

In this test mode, data received from the external codec by the record channel is discarded and replaced by an (8-bit) incrementing count. This is intended for use in A-law / Mu-law speech mode where the 8-bit codec receive data is passed directly to the host.

9.22.2 Test Mode 2: digital milliwatt

Command: 511DH
Status: 511DH

In this test mode, data received from the external mu-law codec by the record channel is discarded and replaced by the CCITT G.711 A-law / Mu-law digital milliwatt (0 dBm0) code sequence. This is a sequence of 8 repeating bytes (A-law / Mu-law samples) representing a 1 KHz sinewave at 0 dBm0.

9.22.3 Test Mode 3: loopback

Command: 511CH
Status: 511CH

In this test mode, data received from the external codec by the record channel is discarded and replaced by the codec output data from the transmit (playback) channel. The playback channel is not affected by this mode of operation. The playback speech data is also transmitted to the output codec.

Note that receive codec to transmit codec loopback can be performed by the host with the CT8020 operating in normal mode. To do this, the host simply copies mu-law frames from the record (receive) channel back to the playback (transmit) channel.

9.22.4 Exit Test Mode

Command: 511EH
Status: 511EH

This command is used to exit test mode and return the record and playback channels to their normal operating mode.

9.22.5 Codec Loopback

Independently of the test modes described above, the CT8020 also supports codec-input to codec-output loopback. In this mode, every frame period (30 ms), the CT8020 will loop-back 240 samples from the input codec back to the output codec. To enter this mode, the CT8020 must be in the IDLE state. To activate this mode use the command:

Command   = 4000H
Status   = 4000H

This loop-back mode can be used in conjunction with Test Mode 2 above to generate a digital milliwatt output signal to the codec.
Also the Codec Configuration command can be used to select the input and output codecs used for the loop-back operation. For example the following codec routing are possible:

Input Signal From	Output Signal To	Codec Configuration Command	
		OUTPUT CODEC	INPUT CODEC
Codec 1	Codec 1	00	0
Codec 1	Codec 0	10	0
Codec 1	Codec 0 & 1	11	0
Codec 0	Codec 0	10	1
Codec 0	Codec 1	00	1
Codec 0	Codec 0 & 1	11	1

The INPUT CODEC field operates to exchange (swap) the input signals from Codec 0 and Codec 1.

Use of this form of loopback operation requires that the CT8020 is in the IDLE state when the command to activate loopback is issued. This loopback configuration can not be used in conjunction with other CT8020 operational modes (e.g. playback and record). To perform loop-back type operations in record or playback, refer to the section on Codec Monitoring.

To exit loopback mode, the Host should issue the IDLE command (0000H).

9.22.6 Codec (Audio) Monitoring

Codec Monitoring provides a mechanism which allows the input signal at one codec to be monitored (echoed) to the output of either or both codecs. This mechanism operates independently of the primary CT8020 operational modes (e.g. record). This allows the Host to implement "call-screening" type functions where a recording being made via the input from codec 0 can be monitored by the user via the output of codec 1.

Command   = CE1XH
Status   = CE1XH

where X selects the action from the following table

X	Codec Routing Configuration
0	Normal operation This setting must be selected for standalone speakerphone operation
1	Codec 0 input echoed to Codec 0 output and Codec 1 input echoed to Codec 1 output
2	Codec 0 input echoed to Codec 1 output and Codec 1 input echoed to Codec 0 output
3	Codec 0 input echoed to Codec 0 and Codec 1 output
4	Codec 1 input echoed to Codec 0 and Codec 1 output

The codec routing described here is over-ridden by the values selected for INPUT CODEC and OUTPUT CODEC in the Codec Configuration command. For example, setting CODEC INPUT to '1' will reverse the Codec input entries in the table above.

For any operations involving playback or tone generation, X should be set to zero.

9.23 Power Save Modes

9.23.1 CT8020 Stop Mode

The CT8020 can be placed into Stop Mode using the command:

Command: 0FF0H

Since the CT8020 halts all internal operations in response to this command, there is no status response.

The CT8020 can only be released from Stop mode using the external RESET pin. After reset, the CT8020 performs internal initializations and then asserts the Control Ready bit in the Hardware Status Register. The Host must wait for the Control Ready bit to be set before issuing the first command. Following reset, the Host must re-program the codec configuration before attempting any other operations.

In stop mode, the codec signals FSYNC and SCLK are also stopped.

9.23.2 Stop Codec Mode

Command: 0FF2H
Status: 0FF2H

In Stop Codec mode, the CT8020 FSYNC and SCLK output pins are forced low. Holding FSYNC low and stopping SCLK, will cause some CODECs to enter power down mode. See your codec data sheet to see if this feature is supported.

To achieve maximum system power saving, the codec interface should be placed in stop mode before placing the CT8020 itself in stop mode. Following this sequence will guarantee that FSYNC halts in the low state.

9.23.3 Re-Start Codec

The codec can be restarted using the command:

Command: 0FF3H
Status: 0FF3H

9.23.4 CT8020 Slow Down (Power Save) Modes

The CT8020 can be programmed by the host into slow down mode. In slow down mode, the clock rate of the internal DSP core is reduced to allow just sufficient processing power for the operation selected. For example, when the CT8020 is performing Full Duplex TrueSpeech 6.3 operation in conjunction with AEC operation, the DSP core must be run at full speed. But when the CT8020 is being used in pass through mode to playback un-compressed 16-bit linear data, the DSP core can be operated at greatly reduced speed.

To enter slow-down mode use the following command:

Command   = 0FEXH   where X is the internal DSP clock division factor (CLK_RATE)
Status   = 0FEXH

The internal DSP core clock is divided by (X+1), such that:

X=0 selects full speed
X=1 selects half speed
X=2 selects one third speed
X=3 selects one quarter speed
X=F selects one sixteenth speed

The internal DSP clock frequency can be observed on the CLKOUT pin.

The following table gives an approximate guide to the processing speed required for some example operations:

Operation	X value	DSP internal speed factor	Typical Power Consumption
Full Duplex TrueSpeech 6.3-4.1 + AEC	0	1.0	260 mA
Full Duplex TrueSpeech 8.5 + AEC	1	1/2	140 mA
Playback only (all modes)	3	1/4	80 mA
Full Duplex un-compressed speech	3	1/4	80 mA
Line Monitoring (tone detection)	3	1/4	80 mA
IDLE	F	1/16	40 mA

AEC = Acoustic Echo Canceller

9.24 General Purpose Input Output pins (GPIO)

The CT8020 provides 8 GPIO pins, GPIO-0 to GPIO-7. Three of these pins are normally reserved for use by the CT8020 internal firmware:

GPIO-0 is used to provide the DATAFLAGN output signal
GPIO-4 is a system reserved output
GPIO-5 is used to provide the frame interrupt output signal

These pins are automatically configured as outputs at reset time by the CT8020. The remaining 5 GPIO pins are configured as inputs and are available for use by the Host.

9.24.1 Configure GPIO input/output direction:

Command = 09XXH

0000 1001	GPIO-7	GPIO-6	X	X	GPIO-3	GPIO-2	GPIO-1	X
(15-8)	(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)

Status = 09XXH

0000 1001	GPIO-7	GPIO-6	1	1	GPIO-3	GPIO-2	GPIO-1	1
(15-8)	(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)

setting the GPIO bit to '1' configures the pin as an output, setting the bit to '0' configures the pin as an input.

9.24.2 Write GPIO pins

Command = 0BXXH

0000 1011	GPIO-7	GPIO-6	X	X	GPIO-3	GPIO-2	GPIO-1	X
(15-8)	(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)

Status = 09XXH

0000 1011	GPIO-7	GPIO-6	FRN	X	GPIO-3	GPIO-2	GPIO-1	DATA FLAG
(15-8)	(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)

The status response echoes the GPIO bit values in the 0BXXH commands. Regardless of the GPIO direction configured, the status echoes the value echoes the value written in the 0BXXH command. If the pin is an input, it is not affected by this operation. Bits 0, 4 and 5 of the status response show the current state of the CT8020 reserved output bits.

9.24.3 Read GPIO pins

Command = 5143H (this is the Read FR - frame interrupt command)

0101	0001	0100	0011
(15-12)	(11-8)	(7-4)	(3-0)

Status = YYXXH

GPIO-7	GPIO-6	GPIO-5	GPIO-4 FRN	GPIO-3 reserved	GPIO-2	GPIO-1	GPIO-0 DATA-FLAG
(read)	(read)	(read)	(read)	(read)	(read)	(read)	(read)
(15)	(14)	(13)	(12)	(11)	(10)	(9)	(8)

GPIO-7	GPIO-6	GPIO-5	GPIO-4 FRN	GPIO-3 reserved	GPIO-2	GPIO-1	GPIO-0 DATA-FLAG
(readback)	(readback)	(readback)	(readback)	(readback)	(readback)	(readback)	(readback)
(7)	(6)	(5)	(4)	(3)	(2)	(1)	(0)

The m.s. 8-bits "YY" of the status response show the state of the GPIO input pins.

The l.s. 8-bits "XX" of the status response show the last data written to the GPIO pins (readback).

If the GPIO pin is configured as an input, the state of the input pin is reflected in the matching bit in the YY upper byte of the status reply. The matching bit in the XX lower byte shows the last value written to the pin. This "readback" value will control the state of the pin if the direction bit is changed to program the pin as an output. This represents the "potential" state of the pin should it be changed to an output.

If the GPIO pin is configured as an output, the state of the pin as sensed by the GPIO hardware will be reflected in the YY upper byte (reading the state of the actual output pin). The last value actually written to the pin will be shown in the XX lower byte. Under normal circumstances, the bit value in XX and YY will match. Only under abnormal circumstances, for example a short circuit to ground, will the XX and YY bit states be different.

This is also the command shown in the FRAME INTERRUPT section of this data sheet, used for reading the state of the Frame Interrupt pin (FRN).

10. CT8020 Host Interface Timing

## *10.1 Host Write to Software Control Register m.s. byte*
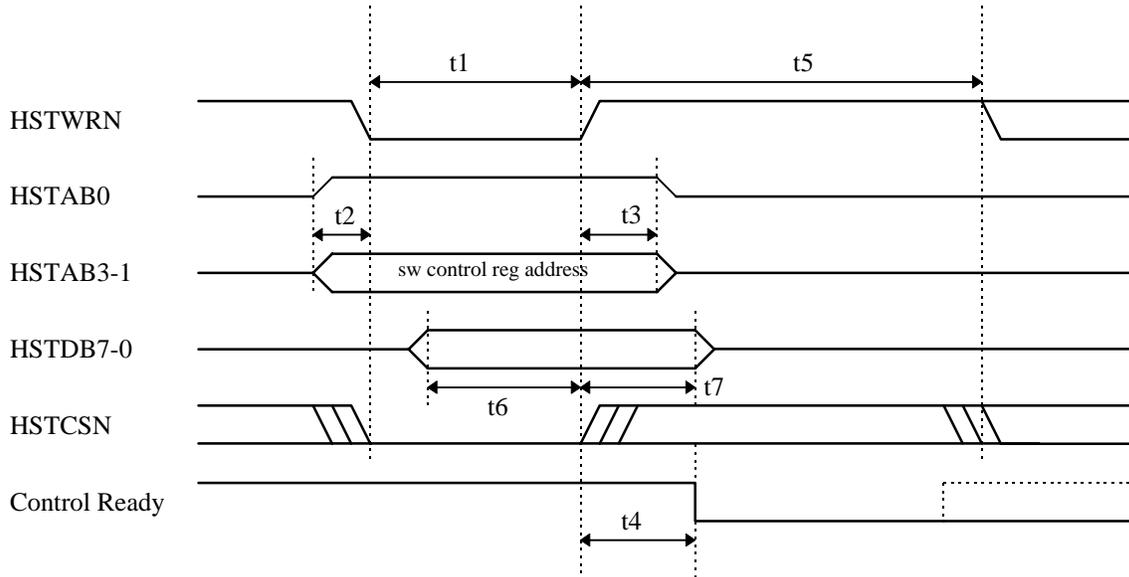
Parameter	Description	Min	Max
t1	HSTWRN pulse width	2 * MAINCLOCKP	
t2	HSTAB3-0 setup time before falling edge of HSTWRN or HSTCSN	5 ns	
t3	HSTAB3-0 hold time after rising edge of HSTWRN or HSTCSN	2 ns	
t4	Delay from rising edge of HSTWRN or HSTCSN to Control Ready cleared		MAINCLOCKP
t5	Recovery time between Host accesses	2 * MAINCLOCKP	
t6	HSTDB7-0 setup time before rising edge of HSTWRN or HSTCSN	20 ns	
t7	HSTDB7-0 hold time after rising edge of HSTWRN or HSTCSN	5 ns	

Notes:
1. Host writes to m.s. byte of Software Control Register

2. Same timings apply to writes to Aux Control Register
3. Control Ready (or Aux Control Ready) cleared by Host Write to Software Control Register (or Aux Software Control Register. Control Ready bit visible to Host in Hardware Status Register. Must be valid in time for read by next host access.
4. MAINCLOCKP period = 2/XIN (effective) = 25.0 ns at 40.0 Mips with 4.000 MHz external crystal or 80.000 MHz external clock.
5. t4 may be negative
6. t4 must be less than t5 so that Control Ready is valid for the next host access. The Control Ready signal illustrated is the bit visible to the Host in the Hardware Status Register

10.2 Host Read from Software Status Register m.s. byte
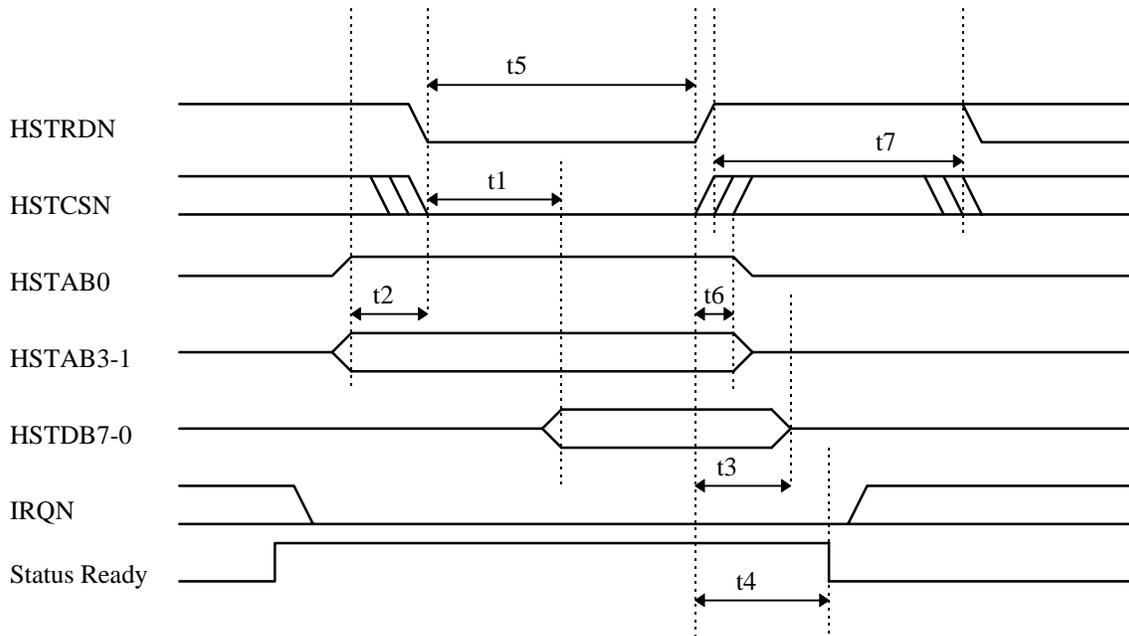
Parameter	Description	Min	Max
t1	HSTRDN or HSTCSN to data out valid		30 ns
t2	HSTAB3-0 setup time before falling edge of HSTRDN or HSTCSN	5 ns	
t3	HSTRDN or HSTCSN inactive to data out tri-state (output disable delay)		30 ns
t4	HSTRDN or HSTCSN positive edge to Status Ready clear		MAINCLOCKP
t5	HSTRDN or HSTCSN width	2 * MAINCLOCKP	
t6	HSTAB3-0 hold time after positive edge of HSTRDN or HSTCSN	2 ns	
t7	Recovery time between Host Accesses	2 * MAINCLOCKP	

Notes:
1. Internal DSP WRITE to Software Status Register (or Aux Software Status Register) sets Status Ready bit in Host Hardware Status Register
2. IRQN asserted to Host assumes that the appropriate IE bit is set in the Host Hardware Control Register
3. Host read of Software Status Register m.s. byte clears Status Ready bit, de-asserts IRQN. The Status Ready bit illustrated is the bit that is visible to the Host in the Hardware Status Register.
4. t4 maybe negative.

10.3 Host Write to Host Transmit Data Buffer Access Port

byte 1   byte 2   byte 2N
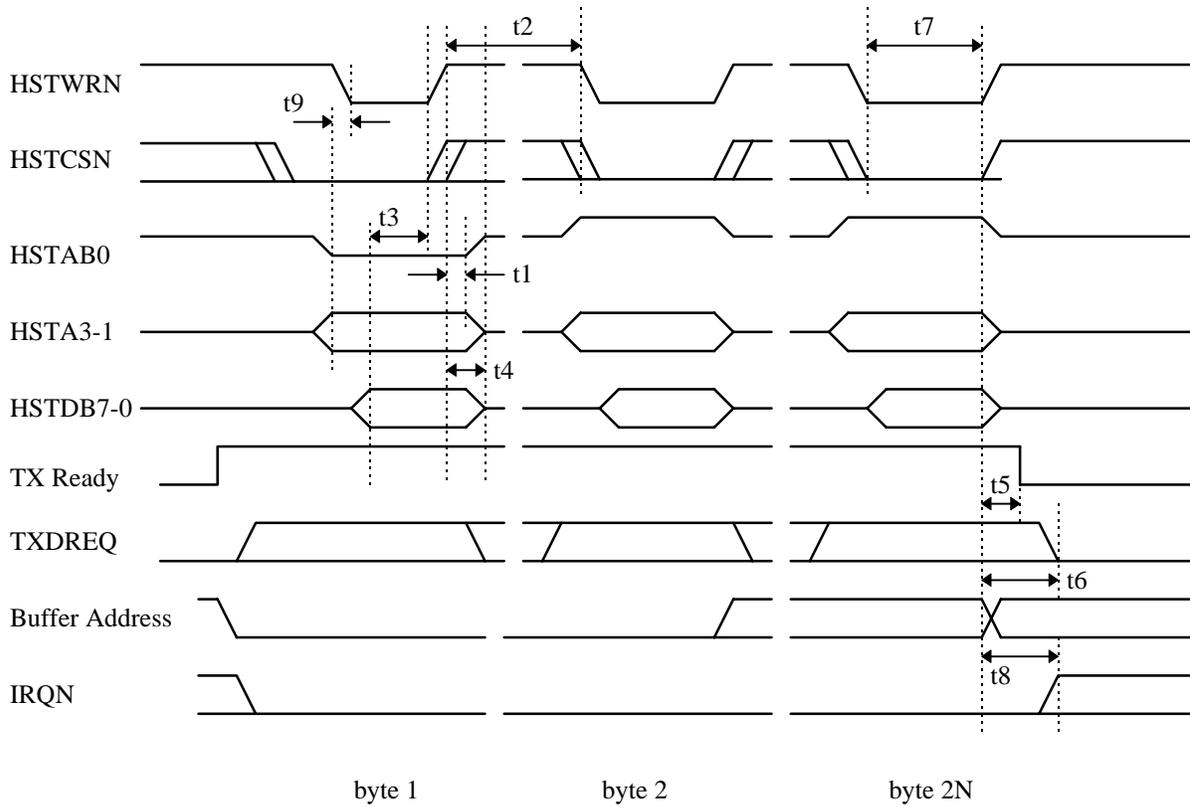
Parameter	Description	Min	Max
t1	HSTAB0-3 hold time after rising edge of HSTWRN or HSTCSN	2 ns	
t2	Recovery time between Host accesses	2 * MAINCLOCKP	
t3	HSTDB7-0 setup time before rising edge of HSTWRN or HSTCSN	20 ns	
t4	HSTDB7-0 hold time after rising edge of HSTWRN or HSTCSN	5 ns	
t5	Final rising edge of HSTWRN to TX Ready cleared		MAINCLOCKP
t6	Final rising edge of HSTWRN to TXDREQ cleared		MAINCLOCKP
t7	HSTWRN width	2 * MAINCLOCKP	

t8	Final rising edge of HSTWRN to IRQN de-asserted		MAINCLOCKP
t9	HSTAB3-0 valid before HSTWRN asserted	5 ns	

Notes
1. Internal Buffer Address cleared by transition of TX Ready bit from 0 to 1
2. Internal Buffer Address increments on rising edge of HSTWRN only if HSTAB0 = 1
3. TX Ready bit clears on final HSTWRN after N access with HSTAB0 =1, where N is the Frame Size value (word count).
4. TXDREQ asserted if TX DMA Enable bit is set in the Hardware Control Register.
5. TXDREQ may operate in Burst Mode or Single Cycle Mode.
6. IRQN driven by TX Ready if TX Ready IE bit set in Host Hardware Control Register.
7. t5, t6 and t8 may be negative

10.4 Host Read From Host Receive Data Buffer Access Port
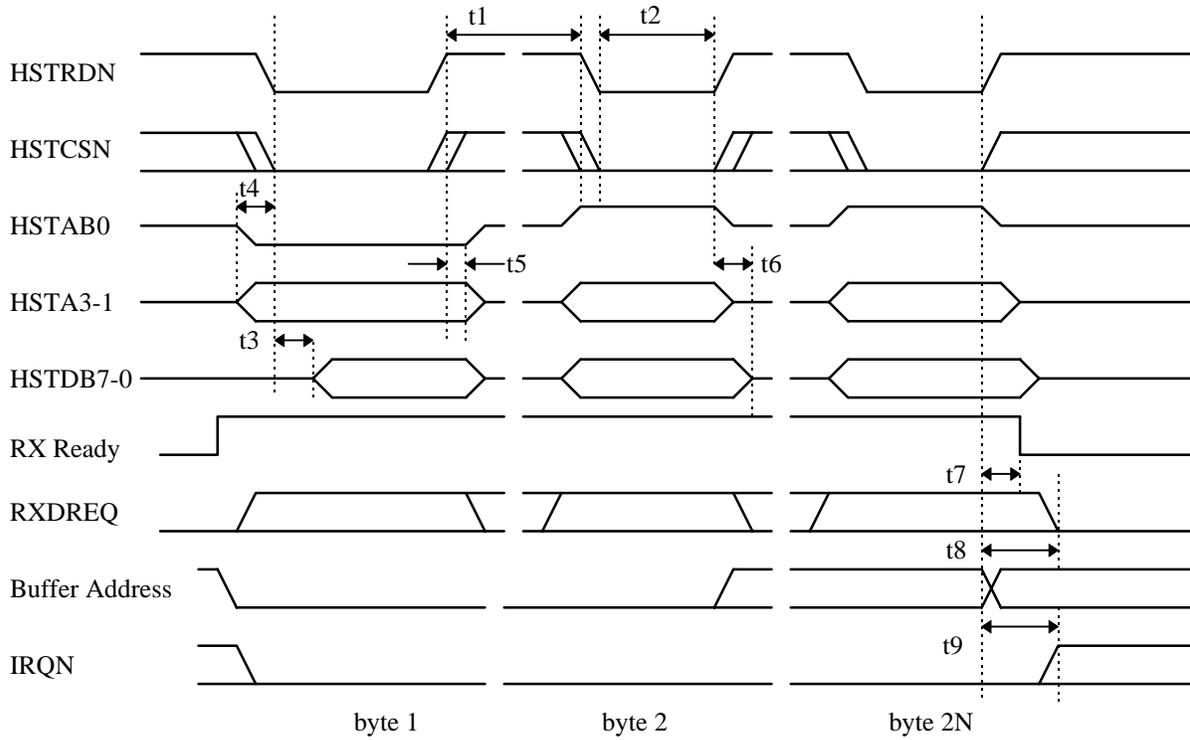
Parameter	Description	Min	Max
t1	Recovery time between Host accesses	2 * MAINCLOCKP	
t2	HSTRDN width	2 * MAINCLOCKP	
t3	HSTRDN or HSTCSN to data out valid		30 ns
t4	HSTAB3-0 setup time prior to falling edge of HSTRDN or HSTCSN	5 ns	
t5	HSTAB3-0 hold time after positive edge of HSTRDN or HSTCSN	2 ns	
t6	HSTRDN or HSTCSN inactive to data out tri-state (output disable delay)		30 ns

t7	Final rising edge of HSTRDN to RX Ready cleared		MAINCLOCKP
t8	Final rising edge of HSTRDN to RXDREQ cleared		MAINCLOCKP
t9	Final rising edge of HSTRDN to IRQN de-asserted		MAINCLOCKP

Notes:
1. Internal Buffer Address cleared by transisition of RX Ready bit from 0 to 1.
2. Internal Buffer Address increments on HSTRDN only if HSTAB0 = 1.
3. RX Ready bit clears on final HSTRDN after N accesses with HSTAB0=1, where N is the Frame Size value (word count).
4. RXDREQ asserted if DMA enable bit is set in the Hardware Control Register.
5. RXDREQ may operate in Burst Mode or Single Cycle Mode.
6. IRQN driven by RX Ready if RX Ready IE bit is set in the Host Hardware Control Register.
7. t7, t8, t9 may be negative

10.5 DMA Write to Host Transmit Data Buffer Access Port (Burst Mode)
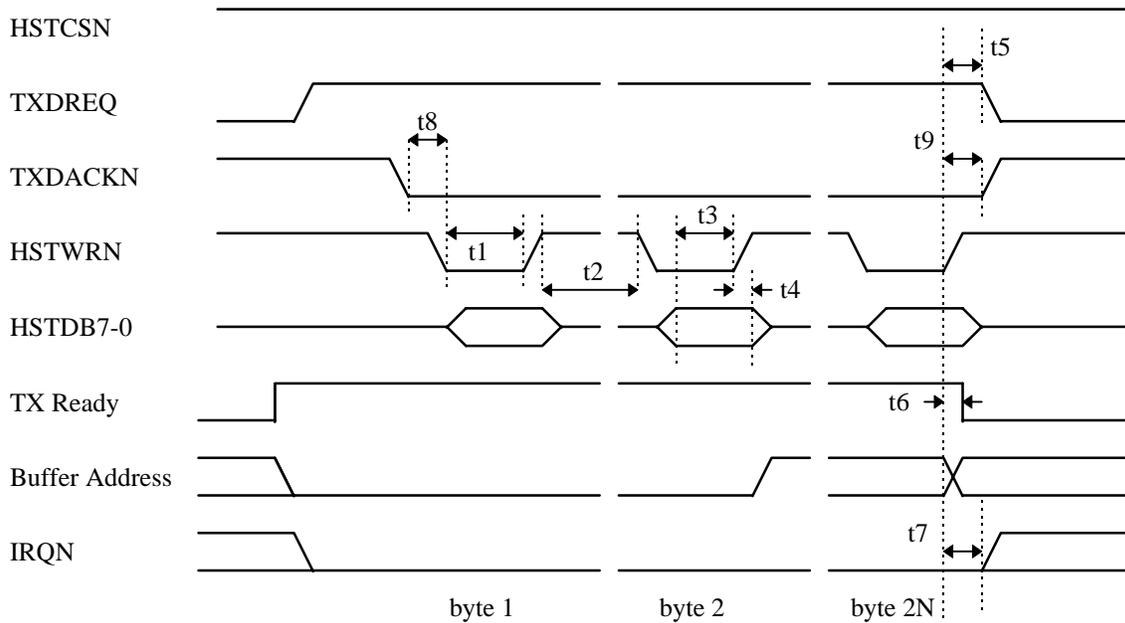
| Parameter	Description	Min	Max
t1	HSTWRN width	2 * MAINCLOCKP	
t2	Recovery time between Host accesses	2 * MAINCLOCKP	
t3	HSTDB7-0 setup time before rising edge of HSTWRN	20 ns	
t4	HSTDB7-0 hold time after rising edge of HSTWRN	5 ns	
t5	TXDREQ de-asserted after final rising edge of HSTWRN		MAINCLOCKP
t6	Final rising edge of HSTWRN to TX Ready cleared		MAINCLOCKP
t7	Final rising edge of HSTWRN to IRQN cleared		MAINCLOCKP
t8	TXDACKN asserted before HSTWRN	5 ns	
t9	TXDACKN hold time after rising edge of HSTWRN	2 ns	

Notes:
1. t5, t6, t7 may be negative

10.6 DMA Write to Host Transmit Data Buffer Access Port (Single Cycle Mode)

HSTCSN				
TXDREQ	t1		t2	
TXDACKN				t4
HSTWRN		t3		
HSTDB7-0				
TX Ready				
Buffer Address				
IRQN				

byte 1   byte 2   byte 2N
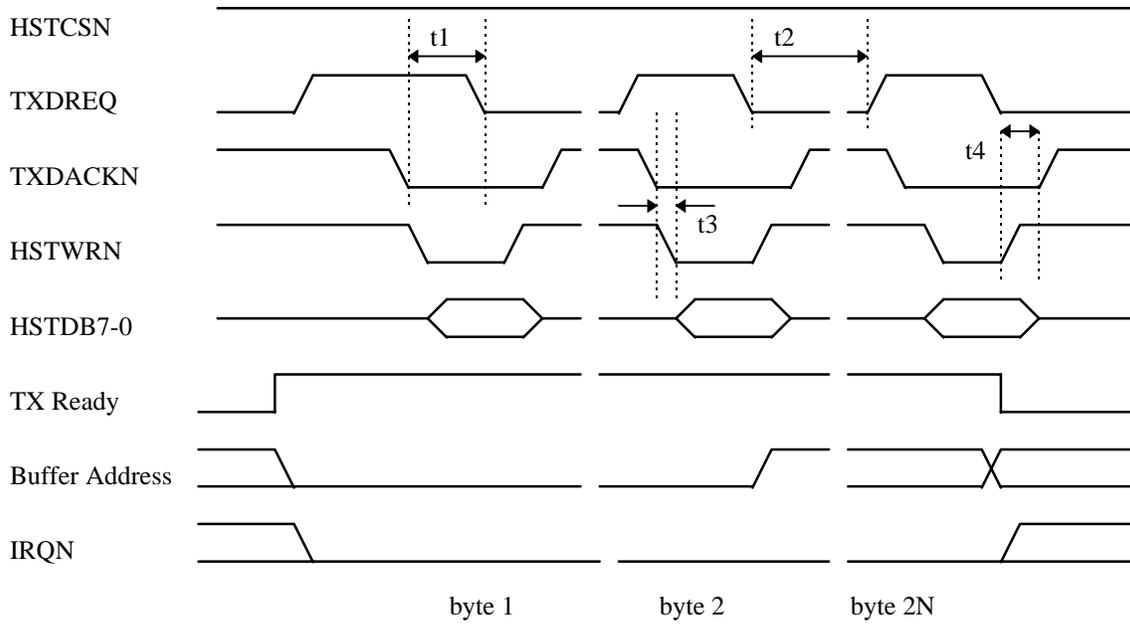
Parameter	Description	Min	Max
t1	TXDACKN asserted to TXDREQ de-asserted response time		3 * MAINCLOCKP
t2	TXDREQ re-assertion delay	16 * MAINCLOCKP	
t3	TXDACKN setup time before falling edge of HSTWRN	5 ns	
t4	TXDACKN hold time after rising edge of HSTWRN	2 ns	

10.7 DMA Read from Host Receive Data Buffer Access Port (Burst Mode)
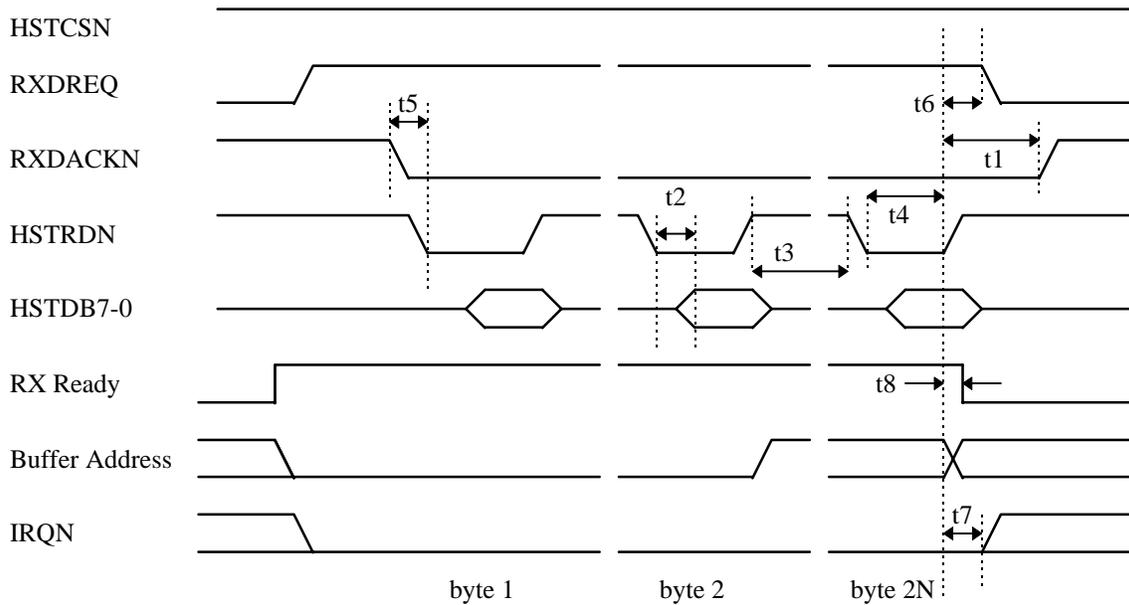
Parameter	Description	Min	Max
t1	RXDACKN hold time after rising edge of HSTRDN	2 ns	
t2	HSTRDN to data valid delay (access time)		30 ns
t3	Recovery time between DMA accesses	2 * MAINCLOCKP	
t4	HSTDRN width	2 * MAINCLOCKP	
t5	RXDACKN setup time before falling edge of HSTRDN	5 ns	
t6	Final rising edge of HSTRDN to RXDREQ de-assertion		MAINCLOCKP
t7	Final rising edge of HSTRDN to IRQN de-assertion		MAINCLOCKP
t8	Final rising edge of HSTDRN to RX Ready de-assertion		MAINCLOCKP

Notes:
1. t6, t7, t8 may be negative

10.8 DMA Read from Host Receive Data Buffer Access Port (Single Cycle Mode)

		byte 1	byte 2	byte 2N
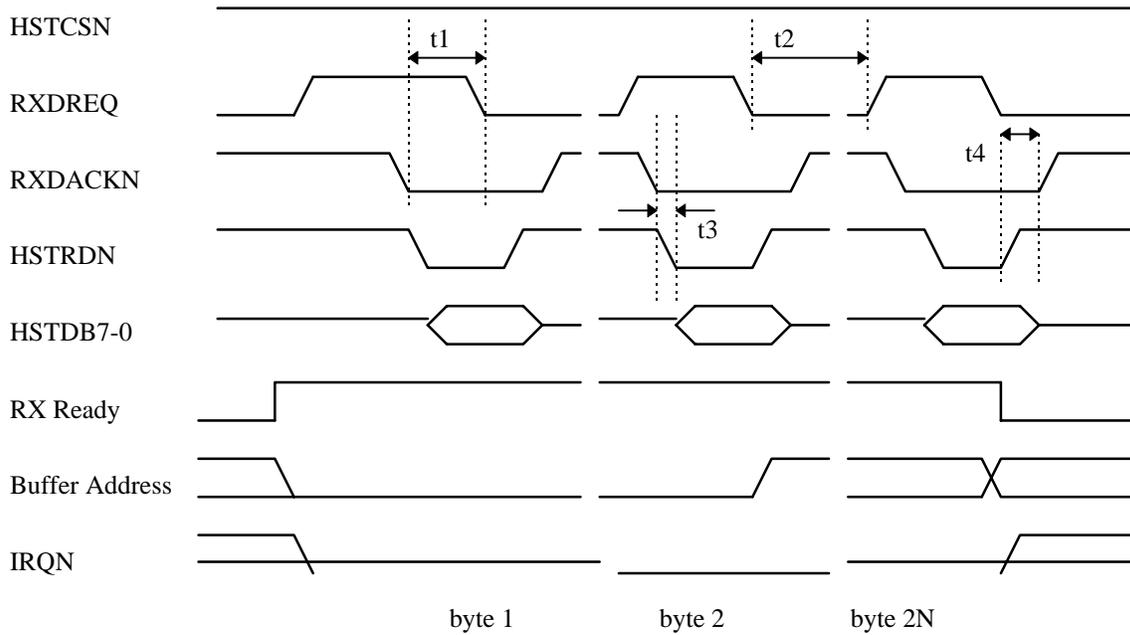
| Parameter	Description	Min	Max
t1	RXDACKN asserted to RXDREQ de-asserted response time		3 * MAINCLOCKP
t2	RXDREQ re-assertion delay	16 * MAINCLOCKP	
t3	RXDACKN setup before falling edge of HSTRDN	5 ns	
t4	RXDACKN hold time after rising edge of HSTRDN	2 ns	

## 11. CT8020 Codec Interface Timing and AC Specification

11.1 Short Frame Sync

Parameter	Description	Min	Max
t1	Output delay from rising edge of SCLK to rising edge of FSYNC (master mode only)	0 ns	50 ns
t2	FSYNC setup time before falling edge of SCLK (slave mode only)	50 ns	
t3	FSYNC hold time after falling edge of SCLK. (slave mode only)	100 ns	
t4	SCLK rising edge to data output valid	0 ns	30 ns
t5	data in setup prior to falling edge od SCLK	30 ns	
t6	data in hold time after falling edge of SCLK	30 ns	
t7	data out tristate after final falling edge of SCLK	0.25 * SCLKPERIOD (122 ns at 2.048 MHz)	0.5 * SCLKPERIOD (244 ns at 2.048 MHz)
t8	FSYNC width (master mode only)		1 SCLK period (nominal)
	SCLK duty cycle	45%	55%

Notes
1. SCLK is 2.048 MHz nominal, SCLKPERIOD is 488 ns nominal
2. Timing diagram shows 8-bit mode only. In 16-bit mode, 16 bits of transmit data are shifted into and out of the CT8020. Bit 15 occurs first.

11.2 Long Frame Sync

Parameter	Description	Min	Max
t1	Output delay from rising edge of SCLK to rising edge of FSYNC (master mode only)	0 ns	50 ns
t2	FSYNC setup time before falling edge of SCLK (slave mode only)	50 ns	
t3	FSYNC hold time after falling edge of SCLK. (slave mode only)	100 ns	
t4	SCLK rising edge to data output valid	0 ns	30 ns
t5	data in setup prior to falling edge od SCLK	30 ns	
t6	data in hold time after falling edge of SCLK	30 ns	

t7	data out tristate after final falling edge of SCLK	0.25 * SCLKPERIOD (122 ns at 2.048 MHz)	0.5 * SCLKPERIOD (244 ns at 2.048 MHz)
t8	FSYNC width master mode		8 SCLK periods in 8-bit mode (nominal). 16 SCLK periods in 16-bit mode (nominal).
	slave mode	1 SCLK period	
t9	ms data bit valid from rising edge of FSYNC. (slave mode only - output enable delay from FSYNC)	0 ns	30 ns
	SCLK duty cycle	45%	55%

Notes
1. SLCK is nominally 2.048 MHz
2. Timing diagram shows 8-bit mode only. In 16-bit mode, 16 bits of data are shifted out of, or into the CT8020. Bit 15 is shifted first.
3. In master mode, FSYNC is 8 SCLK wide (8-bit mode) or 16 SCLK wide (16-bit mode)
4. In slave mode, FSYNC acts as an output enable for DX0,DX1 for the ms data bit during the first SCLK period. (There is no internal synchronization delay on the first bit)
5. In slave mode, once the FSYNC signal has been present for one SCLK falling edge, the internal output enable for DX0 and DX1 is latched and remains active for the appropriate number of SCLK periods. The DX0 and DX1 outputs remain enabled, regardless of the state of FSYNC until following the final SCLK falling edge.
6. In master mode, where FSYNC is an output, it may be used as a tri-state control for gating the receive data. FSYNC will not be de-asserted by the CT8020 until the least significant receive data bit has been latched internally.

12. ELECTRICAL CHARACTERISTICS

Absolute maximum ratings over specified temperature range

Supply voltage range, VCC	-0.3 V to 6 V
Input voltage range	-0.3 V to 6 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-55°C to 150°C

Recommended operating conditions

PARAMETERS	MIN	TYP	MAX	UNIT
V_{CC} supply voltage	4.5	5	5.5	V
V_{SS} supply voltage		0		V
V_{IH} high-level input voltage (all digital input pins except RESET)	2			V
V_{IL} low-level input voltage (all digital input pins except RESET)			0.8	V
VT+ positive going RESET threshold (at VCC = 5.0 v)		3.35	4.6	V
VT- negative going RESET threshold	1.3	1.9		V
I_{OH} high level output current			+4	mA
I_{OL} low level output current			-4	mA
Oscillator crystal (100 ppm) Note the 3.8912 MHz crystal frequency is required only if the CT8020 is to operate in codec master mode and generate a SCLK signal at exactly 2.048 MHz. Otherwise use of a 4.0 MHz crystal is recommended. Operation at 4.0 MHz provides an SCLK at 2.000 MHz.		3.8912	4.000	MHz
T_A operating free-air temperature	0		70	°C

The following circuit is recommended for driving the CT8020 RESET pin in order to meet the VIH spec for this pin:
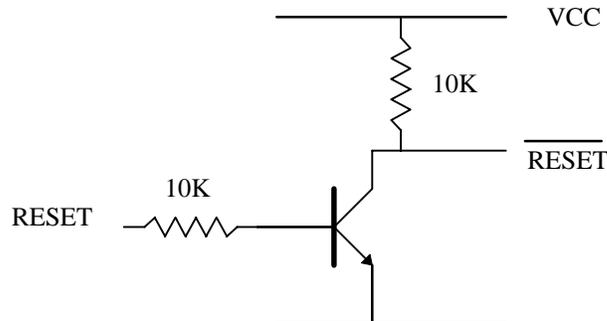
**Electrical characteristics over recommended operating free-air temperature range
(unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH} high level output voltage		VCC = 5V	2.4			V
V_{OL} low level output voltage					0.6	V
I_{OZ} off state output current		VCC = Max			20	μA
I_I input current (pins without pull down resistors)					±20	μA
I_I input current (pins with pull down resistors)					+20 -60	μA
ICC Supply Current	Operating Mode	f = 40 Mips		260	280	mA
	Stop Device Mode	VCC = 5V		0.5	2	mA
	No Clock 25 °C all inputs GND all outputs NC	VCC = 5V		50		uA
CI Input capacitance					20	pF

DTMF & Tone Generation Characteristics

PARAMETER	MIN	TYP	MAX	UNIT
DTMF twist (high/low tone)		2	±8	dB
Tone generator frequency accuracy	-0.1		+0.1	%fc
Tone generator level*	-24		+6	dB0
Tone generator level accuracy	-0.5		+0.5	dB

* 0 dB0 is 0.707 Vrms programmable with 2 dB resolution. Assumes FSYNC = 8.000 KHz

Acoustic echo cancellor performance

PARAMETER		NOTE
Acoustic Echo Cancellation	30 dB	1
Max echo delay	10 ms	2,3

Notes:
1. The acoustic echo cancellor acheives 30 dB of cancellation for white noise in less than 1.0 seconds with the speaker codec output connected to the microphone codec input via a 2:1 attenuator and an output level equivalent to -10 dBm0.
2. The acoustic echo cancellor can cancell echos up to 10 ms (approximately 3.4 meters or 11 feet in sound propagation.
3. Assumes operation of codec at 8.0 KHz sample rate

Electrical echo cancellor performance

| PARAMETER		NOTE
Training pulse duration	16ms	1
Echo duration	23.25ms	1
Canceler length	7.38 ms	1,2
Training pulse peak amplitude	350 mV	3
Training pulse average peak amplitude	250 mV	3
Electrical echo cancellation	34 dB	4

Notes:
1. Assumes operation of codec at 8.0 KHz sample rate.
2. The electrical echo cancellor will model the impulse response of the attached line curcuit for an impulse response up to this duration.
3. Measured at the codec output pin using a TP3054 Texas Instruments mu-law codec.
4. The electrical echo cancellor will acheive 34 dB cancellation for white noise with the line codec output short circuit connected to the line codec input.

13. Mechanical Data - CT8020
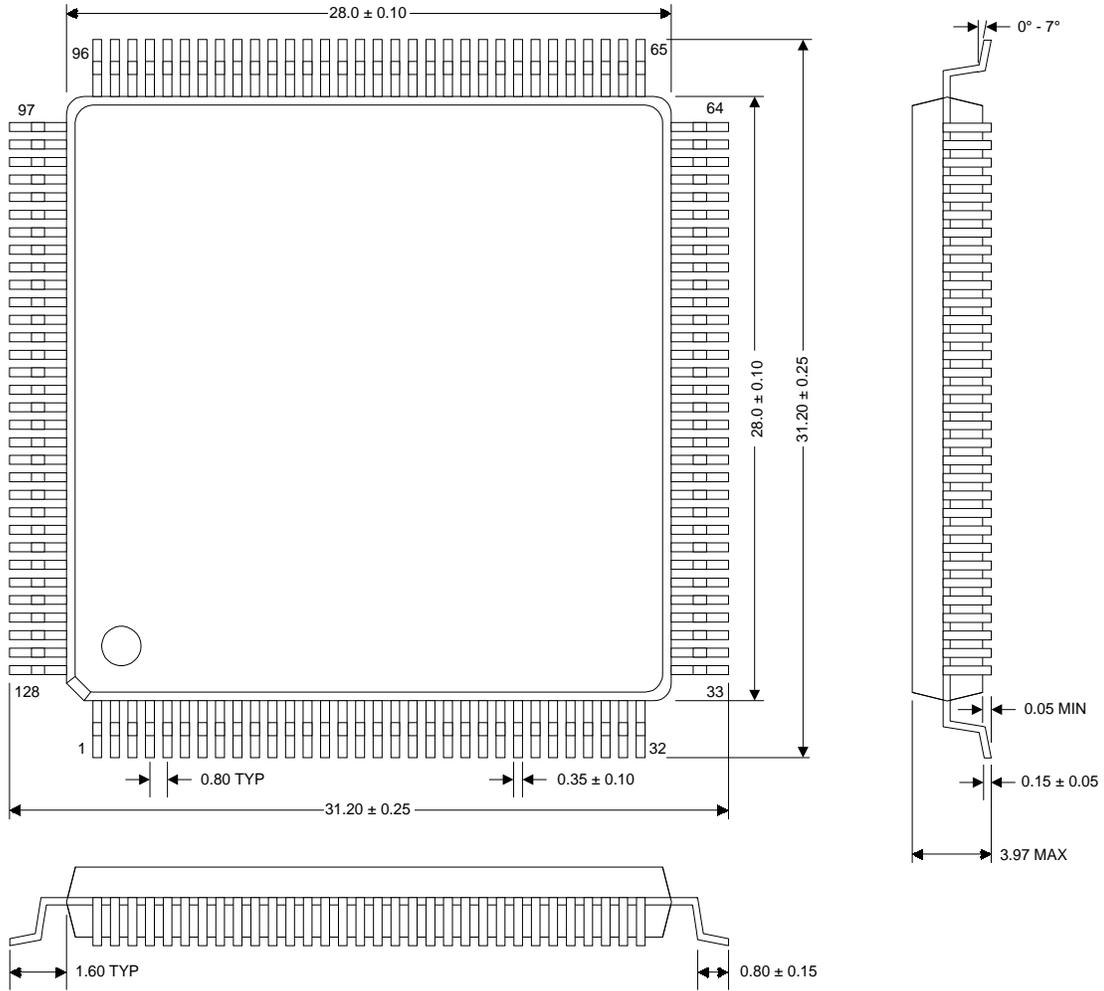
Appendix A : Speakerphone Theory of Operation

SPEAKERPHONE
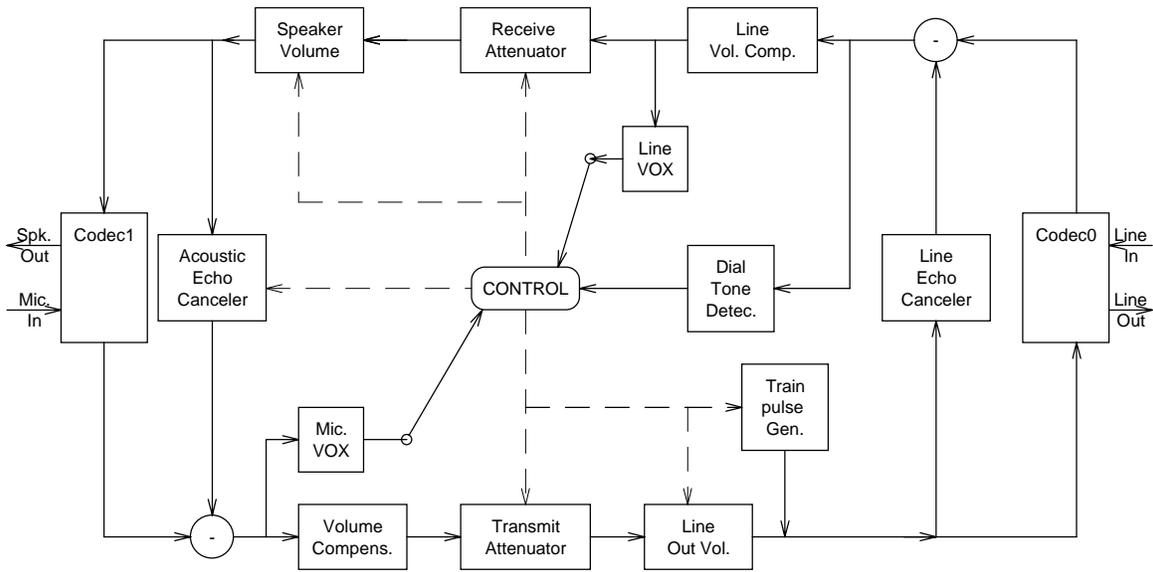
Figure 1.a - Digital part
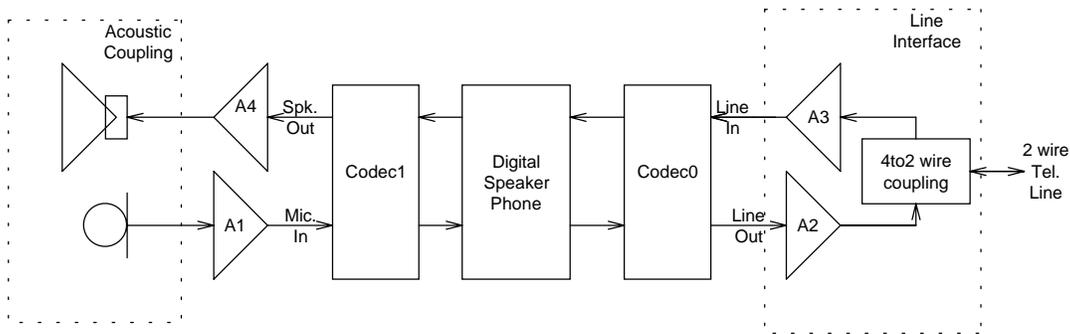
Figure 1.b - Acoustic and analog parts

Introduction

Implementation of a speakerphone system involves three primary sections: external analog circuitry, physical acoustic devices, and the digital canceler (the last, provided by the CT8020). Optimum performance of the speakerphone can only be achieved by correct design and use of all three sections.

Analog Circuitry

The CT8020 interacts with the external physical system via two codecs. Codec0 connects to the telephone line, and Codec1 connects to the microphone and speaker of the speakerphone. The input/output amplifiers (A1-A4) should be configured to make best use of the codecs dynamic range without introducing distortion or clipping of the input/output signals. Care should be exercised in the design of the external circuits to avoid undesirable cross-talk between the various sections. The 4-to-2 wire coupling circuitry at the telephone line interface should be designed to minimize the amount of the outgoing (to line) signal reflected (or echoed) back into the incoming signal (from line). The amount of gain within the loop formed by the amplifiers A1-A4, the 4-to-2 wire coupling, and the microphone-speaker acoustic linkage should be minimized.

The amplifier gains must be selected so that, when the voice signal is coming from the microphone and the telephone line is silent, the signal level at the codec microphone input (codec1) is higher than the reflected signal level at the line codec input (codec0). Also, when the voice signal originates from the telephone line, the input signal at codec0 must be higher than the signal due to the acoustic echo present at the microphone codec1 input. This arrangement allows the CT8020 to determine at any time whether the microphone or line side is speaking. The acoustic echo canceler is only adjusted when the CT8020 determines that the dominant signal is coming from the telephone line side.

Acoustic System

The quality of the microphone and speaker has a direct effect on the level of speakerphone performance attainable. Speech transducers which behave in a non-linear fashion introduce distortions into the signal which can not easily be canceled out. The microphone and speaker should be operated within their linear ranges. Over-driving of either the microphone of speaker must be avoided. Significantly improved performance can be obtained if any physical coupling between the microphone and speaker is eliminated. Ideally, the speaker and microphone should not be housed within the same physical enclosure. Use of a free-standing speaker or microphone, separate from the main system housing is recommended. In a personal computer application, it is often possible to connect to the PC's existing sound system speakers via a sound card's auxiliary input. Use of a free standing external microphone is often more convenient from the users point of view since it allows more flexibility in positioning. Placing of the microphone and speaker such that they are directly facing each other is not recommended. If microphone and speaker are contained within the same physical housing, care should be taken to minimize the physical coupling between them using acoustic isolation materials. In this situation, it is often the case that the physical coupling caused by the housing creates more feedback than the acoustic path. Physical enclosures often exhibit resonances at particular frequencies, these should be damped as much as possible. It is also possible to reduce the effect of these resonances by electrical filtering within the analog circuitry.

CT8020 Digital Canceler

The CT8020 SpeakerPhone system actually contains two digital cancelers: an adaptive acoustical canceler which cancels the acoustic echo between microphone and speaker, and an electrical canceler which cancels the echo caused by the 4-to-2 wire telephone line connection. The CT8020 can be operated in two distinct modes: full duplex mode in which both cancelers are active, and half duplex mode where only the acoustic canceler is used.

Half-Duplex mode

In this half-duplex mode, the loop attenuation selected must be at least 12 dB. In this mode the SpeakerPhone operates by dynamically distributing the loop attenuation selected between the receive and transmit attenuators (see figure 1a). The CT8020 makes a decision as to which direction is talking, and then rapidly shifts the attenuation to the opposite direction. The total attenuation in the loop (receive attenuation plus transmit attenuation) remains constant. The exception to this is when the CT8020 detects abnormal conditions and loop adjustment mode 01 or 10 is selected. Under these circumstances, the CT8020 can (temporarily) introduce an additional 12 dB of attenuation in order to prevent howling or feedback. Abnormal conditions exist when the CT8020 determines that it unable to cancel the acoustic echo by adjusting the echo canceler coefficients. If loop adjust mode 10 is selected, the CT8020 will attempt to restore the original loop attenuation selected by reducing the additional attenuation in steps of 4 dB once the abnormal circumstances are removed.

Half-Duplex mode is the default mode selected when the SpeakerPhone operation is started, before the training pulse has been sent to the telephone line activating the electrical echo canceler. The SpeakerPhone should always be started with a loop attenuation of at least 12 dB. The CT8020 operating in half duplex mode, provides for host selection of the loop attenuation. This gives the system designer some flexibility in design of the external analog circuit. It also provides a more natural sounding speaker phone since the non-talking direction is never entirely muted as with some other speaker phone implementations. Using the lower attenuation levels offered by the CT8020 avoids the un-natural abrupt switching between active directions, present with alternative implementations, which causes the user to experience break up of the conversation.

Full-Duplex mode

In full-duplex mode, the electrical (line-side) echo canceler must be activated by the host micro-controller. When instructed, the CT8020 sends a short duration "training" pulse to the telephone line to measure the echo (impulse) response of the line. This pulse is audible to the user, but is of very short duration and is not intrusive. It is important that there is no incoming signal from the telephone line present when the training pulse is sent. The host micro-controller must determine by some algorithm, the correct time to send the pulse. On an incoming call, the pulse should be sent 100-200 ms after answering the call (going off-hook). This delay allows time for the telephone line conditions to stabilize and for the ringing signal to cease. On an outgoing call, the pulse should be ideally sent around 50ms after dialing the second digit. Again this allows time for the line conditions to have stabilized and avoids interfering with digit detection by the local telephone exchange. Sending the training pulse at this time also helps ensure that the line is silent since at this point no ring tone or busy signal is likely to be present. Sending the training pulse at the end of a speed-dial or re-dial sequence also works well, provided it is sent before ringing tone is presented. Sending the pulse after the first digit is not recommended since it is sometimes the case that a secondary dial tone is encountered (as in dialing 9 for an outside line). The host can determine if training was successful by using the Get Electrical Echo Canceler Quality Factor command. The value of this parameter indicates the degree to which echoes from the telephone line are being canceled. The precise threshold value which indicates

success or failure, depends to an extent on the design and amount of gain of the external hardware. Once the electrical echo canceler has been successfully trained, the loop attenuation can be safely reduced to zero or one of the other full-duplex attenuation factors. Since it is difficult to anticipate all circumstances under which the speakerphone may be used, it is recommended that in addition to the automatic training pulse control logic described, that the facility for the user to manually send the pulse is provided. The speakerphone system should provide a manual speakerphone reset push button that the user can press to activate full duplex mode if the automatic control logic fails for any reason.

Volume Control

The CT8020 includes volume control both for the line output level (8 dB range) and speaker output level (28 dB range). The volume should be adjust using the CT8020 rather than by changing external physical gain. In this way the CT8020 is aware of the change in loop gain directly and can internally compensate for it, instead of having to adaptively adjust for the change. The CT8020 also supports speaker and microphone mute.

Dial Tone Detection

The CT8020 includes special handling for constant level tone signals such as dial tone. Signals of this nature are ignored by the voice detectors used for controlling the loop attenuation. When a steady tone is detected for a period of approximately 1 second, priority (or minimum attenuation) is automatically switched to the line side so that the user will hear the dial tone at full volume. Without this special handling, the CT8020 would see that both the receive and transmit direction had constant signal energy and so would distribute the loop attenuation equally between the two directions. Under these circumstances, the dial tone level heard by the user would be attenuated.

Performance

The acoustical echo canceler can handle echo delays up to 10 ms (approximately 3.4 meters or 11 feet in sound propagation). The canceler gives 34 dB cancellation for white noise in less than 0.5 seconds with the speaker codec output short circuit connected to the microphone codec input.

The electrical echo cancellor generates a training pulse of 16 ms duration with an instantaneous peak output voltage of 350 mV. The maximum line echo duration that will be canceled is 23 ms. With the output codec signal short circuit connected to the input codec signal, the electrical echo cancellor achieves 34 dB of cancellation (measured with white noise). In this test, the echo cancellor performance is primarily limited by the quantization noise associated with the D-to-A and A-to-D translations performed by the mu-law codec.

Example Control Algorithm

This example is provide for illustrative purposes only, system designers are free to construct their own control algorithms as desired.

On detection of an incoming call (off-hook preceded by ringing signal), the host controller should start the speaker phone in half-duplex mode. The host should then wait around 200 ms following the off hook transition before sending the electrical echo canceller training pulse to allow the line conditions to stabilize. After the training pulse has been sent, the host should interrogate the CT8020 to determine if electrical echo cancellor training was successful. If not the host should attempt re-training at 500 ms intervals for a total of 3 attempts. If training is not successful after 3 attempts, the host should continue to let the speaker phone operate in half duplex mode. Training will only fail if there is excessive noise present on the telephone line at the instant that the CT8020 attempts to send the training pulse. As an option, the system designer can provide a manual training or "reset" button to the user, so that the user can decide when the training pulse is sent.

On an outgoing call (e.g. speed dial), the host again starts the speaker phone in half duplex mode. After dialing of the second digit, the host should wait 50 ms and then attempt to send the training pulse. Once the training pulse has been sent, the host can check the success or otherwise of the training process. If training fails, the host can try to train the electrical echo cancellor after the third and subsequent digits until adequate training is achieved. In the event that training is not possible, the host can allow the speaker phone to continue operation in half duplex mode. Sending the training pulse after the second digit is recommended since in many installations, a secondary dial tone may be presented after dialing of the first digit (for example dialing 9 for an external (public network) line).

Training needs to be successfully achieved only once in the duration of any call, provided that the physical line conditions do not change. An example of a change that would require re-training is the situation where a second telephone goes off-hook and is operated in parallel with the original telephone.

Note that true full duplex operation will only be achieve after the electrical echo cancellor has successfully trained and the acoustic echo cancellor has had time to self-adjust. The acoustic echo cancellor is only updated when the telephone line side is talking and the microphone side is silent. This may require a few seconds. When operated in loop adjustment mode 10 (the recommended setting), the CT8020 compensates for the initial start-up conditions by inserting additional loop attenuation. Once the acoustic echo cancellor has stabilized, the additional loop attenuation is reduced and then removed.

Note that is an implementation where the microphone and speaker are physically separate from each other (this is the preferred implementation), the user should be discouraged from moving either microphone or speaker during a call. When the microphone and speaker change relative positions, the acoustic echo cancellor has to work harder to compensate for the changed acoustic echo path. Under these circumstances, in loop adjustment mode 10, the CT8020 may again introduce temporary extra loop attenuation until the situation re-stabilizes. Also if the user desires to change the volume of the loud speaker, this should be done via the CT8020 controls and not by changing the external speaker amplification.

Appendix B : AEC Performance in DSVD Applications

The CT8020 operates the same AEC algorithm in DSVD mode as Speakerphone mode. Since the AEC cancellor operates on the input signal from the microphone, the effect of the AEC is heard at the far-end, as opposed to near-end of the DSVD communication link. The echo path in a symmetrical CT8020 implementation is shown below:

The performance of the AEC at this end of the link affects the user at the other end of the link.

Speaker / AEC	**CT8020** — TrueSpeech Decompression / TrueSpeech Compression	TrueSpeech Compression / TrueSpeech Decompression — **CT8020** AEC
Microphone		Microphone / Speaker

CT8020's connected via a digital link
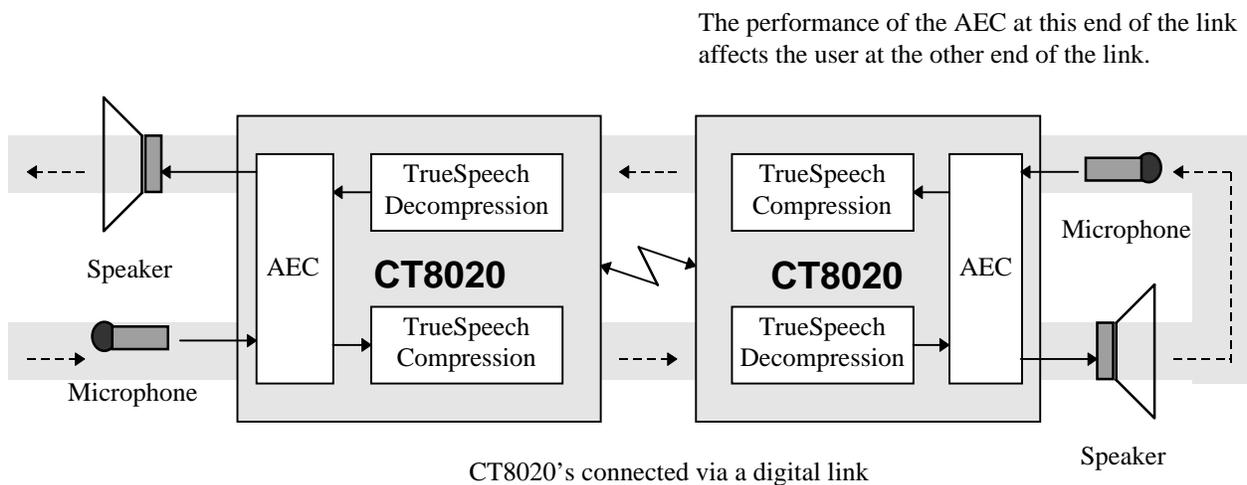
AEC operation in DSVD mode

Under ideal conditions, the AEC can achieve around 34 dB of echo attenuation. With a symmetrical arrangement as above, this can produce up to 68 dB loop (or "round-trip") attenuation. This is more than sufficient to ensure that acoustic feedback , "howling" or "howl-round" does not occur. However the audible echo (attenuated by up to 34 dB) may be overly annoying to users, due to the significant delay that is often present in this type of configuration. The key problem in this environment is the size of the delay, which may be several hundred milliseconds.

When the AEC is active in **speakerphone** mode, the primary consideration is to prevent "howling". This condition is met, when the total loop gain in the system is less than 1.0. The round-trip delay in this mode is very short. With a short delay, the human ear is not able to perceive an echo with 34 dB of attenuation except as a minor reverberation sound effect.

When the AEC is active in **DSVD** mode, since the delay is much greater, the **perceptual response to the same level echo is much greater**. The effect of a user hearing their own words echoed back to them with a 300-500 ms delay is very distracting, even with 34 dB of attenuation. To overcome this problem, it is necessary to introduce additional attenuation into the loop. To this end, it is recommended that the AEC be operated with at least 12 dB of loop attenuation. While this precludes the possibility of operating in "true" full duplex DSVD speakerphone mode, the additional 12 dB of attenuation enables the CT8020 to achieve "near full duplex" operation. In this mode, the CT8020 monitors the receive and transmit directions in order

to decide which direction is talking. It then attenuates the opposite direction by the loop attenuation amount selected. The loop attenuation setting is programmable by the host in steps of 4 dB from 0 to 28 dB. The active switching of attenuation between the two speech directions is usually not noticeable to the user. The "near full duplex" performance of the CT8020 in this mode, still provides superior performance to comparable systems operating in half-duplex mode, where at any time, one speech direction is completely muted. Also note that, without the AEC active in the illustrated situation, "howling" is extremely likely to occur, making the speech link unusable.

The CT8020 may be operated in DSVD mode without the AEC if a handset is used in place of a speaker-microphone arrangement.

Appendix C :: Wave File Format (.wav)

WAVE file format is actually a sub-format of RIFF (Resource Interchange File Format) and is as follows:

Example for 8/16 bit linear data (note - the byte offsets given are for illustration only, the byte offsets in a wave file are not absolute):

byte offset	number of bytes	contents
0000H	4	"RIFF" = 52 49 46 46 (hex)
0004H	4	filesize -8 (the size of the waveform chunk)
0008H	4	"WAVE" = 57 41 56 45 (hex)
000CH	4	"fmt " = 66 6D 74 20 (hex)
0010H	4	format chunk size (16 for linear data)
0014H	2	wFormatTag = 1 (WAVE_FORMAT_PCM)
0016H	2	nChannels (number of channels 1:mono 2:stereo)
0018H	4	nSamplesPerSec (e.g. 8000)
001CH	4	nAvgBytesPerSec (.e.g. 8000, 16000)
0020H	2	nBlockAlign (block size in bytes 8-bit mono:1, 16 bit stereo:4)
0022H	2	wBitsPerSample (e.g. 8 or 16)
0024H	4	"data" = 64 61 74 61 (hex)
0028H	4	waveform data size (bytes)
002CH		start of actual waveform data

Example for TrueSpeech data (note - the byte offsets given are for illustration only, the byte offsets in a wave file are not absolute):

byte offset	number of bytes	contents
0000H	4	"RIFF" = 52 49 46 46 (hex)
0004H	4	filesize -8 (the size of the waveform chunk)
0008H	4	"WAVE" = 57 41 56 45 (hex)
000CH	4	"fmt " = 66 6D 74 20 (hex)
0010H	4	format chunk size = 32H
0014H	2	wFormatTag = 22H (TrueSpeech tag value)
0016H	2	nChannels = 1
0018H	4	nSamplesPerSec = 8000
001CH	4	nAvgBytesPerSec = 1067 (used for buffer size estimation)
0020H	2	nBlockAlign = 20H
0022H	2	wBitsPerSample = 1
0024H	2	cbSize = 20H (size of extension area following)
0026H	2	wRevision = 1 (For TrueSpeech 8.5)
0028H	2	nSamplesPerBlock = 240
002AH	28	abReserved[28] (reserved area)
0042H	4	"fact" = 66 61 63 74
0046H	4	fact chunk size = 4
004AH	4	time length of data in sample units (e.g. 8000 = 1 sec)

004EH	4	"data" = 64 61 74 61 (hex)
0052H	4	waveform data size (bytes)
0056H		start of actual waveform data

Note that all wave formats except WAVE_FORMAT_PCM are required to includes a "fact" chunk which gives the time length of the "data" chunk expressed in samples.

The general format for wave consists of a 4 byte ASCII tag for each chunk ("fmt ", "data") followed by a 4 bytes giving the length of the chunk (not including the 8 byte tag-length header), followed by the actual data for the chunk. A wave file can contain many chunks in any order. An application must search for the chunks it is interested in by skipping over other chunks that it does not understand. For example:

"RIFF"
"WAVE"
"test"
16
16 bytes of "test"chunk data
"fmt "
16
16 bytes of "fmt " data
"data"
1024
1024 bytes of "data"
"more"
32
32 bytes of "more" data

Note that the case of the 4 byte ASCII tag is significant.

When an application encounters the tag "test", it should read the next 4 bytes which contains the length (16) of the "test" chunk, then the application should move forward through the file 16 bytes. This will position the file at the next chunk tag. The application should then read this tag and repeat the above process until it encounters the chunk that it is looking for.

To playback a wave file, the application should first find the "fmt " chunk and determine if it can handle the wave format it describes. Only then should the application search for the "data" chunk to obtain the actual waveform data.

Appendix D :: CT8020 Evaluation Board

The diagram below shows the layout of the CT8020. It indicates the positions of the main components and connectors. The actual EVB may contain locations for additional components. These additional components are not required for operation of the CT8020. They are intended to support operation of other devices in the CT8XXX family. Connector pins are on 0.1 inch pitch.
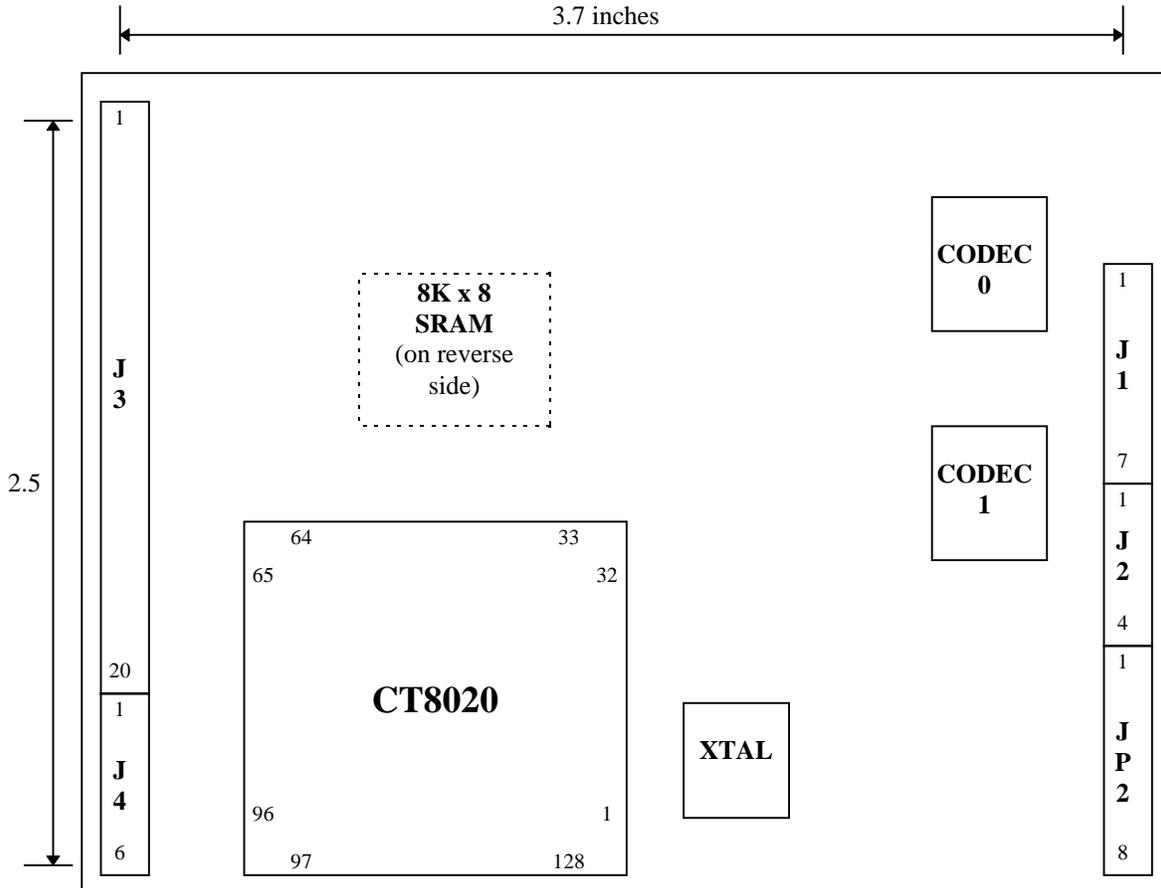
CT8020 Family EVB

The following components that are shown on the **full** EVB schematics were used for development purposes **only** and are not required for normal operation of the CT8020:

external program SRAMs MCM670R-6 (U51,U52,U53,U54)
32K x 8 data SRAM **option** MCM6206-25 (U3)
external EPROM 27010PLCC (U14)
connector JP1

EVB boards normally supplied to customers do not include these additional components. The EVB contains options for either 8Kx8 or 32Kx8 SRAM. Only the 8K x 8 is required, but 32K x 8 may be substituted instead.

The jumper pin connection settings for normal operation are: JP3 2-3, JP4 2-3, JP5 2-3, JP5 2-3, JP12 3-5 4-6

CT8020 EVB Connector Pin Out

J1	
1	AGND
2	Line In
3	AGND
4	Line Out
5	(Line Out-)
6	AGND
7	(Speaker Out-)

J4	
1	
2	GPIO1
3	HSTCSN
4	
5	
6	

J2	
1	AGND
2	Mic In
3	AGND
4	Speaker Out

JP2	
1	HSTAB1
2	HSTAB2
3	HSTAB3
4	TXDACKN
5	TXDREQ
6	GPI05 / FRN
7	RXDREQ
8	RXDACKN

J3	
1	VCC +5V
2	VCC1 +5V
3	HSTDB0
4	HSTDB1
5	HSTDB2
6	HSTDB3
7	HSTDB4
8	HSTDB5
9	HSTDB6
10	HSTDB7
11	HSTAB0
12	HSTRD
13	HSTWR
14	IRQN
15	GPIO0 / DATAFLAGN
16	RESETN
17	GND
18	AGND
19	EXTINTN
20	-5V

THE DSP GROUP INC.

CT8020

CT8020 REFERENCE DESIGN

OPTIONAL

SINGLE GND CONNECTION

ALTERNATE for
CODEC 0 & 1
(Y1 MUST BE CHANGED TO 3.8912MHz)

HOST PORT

GPIO0==DATAFLAGN

DSP GROUP, Inc.

Title

CT8020 REFERENCE DESIGN

Size	Document Number		REV
B			1
Date:	January 14, 1996	Sheet	1	of

Appendix E : G.723.1 Frame Structure

This appendix shows the bit packing scheme used for compressed speech blocks for the G.723.1 6.3 and 5.3 bit rates. Note that the bit packing arrangement has changed from that used by the (pre-release) v3.0 of G.723.1 that was incorporated in the original CT8020A11AQC engineering samples.

The following shows the bit packing used by the CT8020D11AQC for the 6.3 data rate. The compressed speech frame consists of a block of 12 16-bit words. The least significant 2 bits indicate the type of compressed speech block.

LSP Index (low 14 bits)		Vad + Rate
15	2 1	0

Adapt. CodeBook Lag_0:6bits	LSP Index : (high 10 bits)
15 10	9 0

Combined_Gain_0	Adapt.CdBkLag_3	Adapt.CodeBookLag_2:7bits	Adapt.CdBkLag_1	Adapt.CdBk Lag:_0
15 12	11 10	9 3	2 1	0

Combined_Gain_1:8bits	Combined_Gain_0:8bits
15 8	7 0

Combined_Gain_2:12bits	Combined_Gain_1:4bits
15 4	3 0

Grid_3	Grid_2	Grid_1	Grid_0	Combined_Gain_3:12bits
15	14	13	12	11 0

Pulse_Position_0:2bits	Combined_Position_Index:13bits	Reserved Bit
15 14	13 1	0

Pulse_Position_1:2bits	Pulse_Position_0:14bits
15 14	13 0

Pulse_Position_2:4bits	Pulse_Position_1:12bits
15 12	11 0

Pulse_Position_3:4bits	Pulse_Position_2:12bits
15 12	11 0

Pulse_Sign_0:6bits	Pulse_Position_3:10bits
15 10	9 0

Pulse_sign_3:5bits	Pulse_Sign_2:6bits	Pulse_Sign_1:5bits
15 11	10 5	4 0

The following shows the bit packing used by the CT8020 for the 6.3 data rate. The compressed speech frame consists of a block of 12 16-bit words. The least significant 2 bits indicate the type of compressed speech block.

LSP Index (low 14 bits)		Vad + Rate
15	2 1	0

Adapt. CodeBook Lag_0:6bits	LSP Index : (high 10 bits)
15 10	9 0

Combined_Gain_0	Adapt.CdBkLag_3	Adapt.CodeBookLag_2:7bits	Adapt.CdBkLag_1	Adapt.CdBk Lag:_0
15 12	11 10	9 3	2 1	0

Combined_Gain_1:8bits	Combined_Gain_0:8bits
15 8	7 0

Combined_Gain_2:12bits	Combined_Gain_1:4bits
15 4	3 0

Grid_3	Grid_2	Grid_1	Grid_0	Combined_Gain_3:12bits
15	14	13	12	11 0

Pulse_Position_1:4bits	Pulse_Position_0:12bits
15 12	11 0

Pulse_Position_2:8bits	Pulse_Position_1:8bits
15 8	7 0

Pulse_Position_3:12bits	Pulse_Position_2:4bits
15 4	3 0

Pulse_Sign_3:4bits	Pulse_Sign_2:4bits	Pulse_Sign_1:4bits	Pulse_Sign_0:4bits
15 12	11 8	7 4	3 0

G.723.1 Version History

The CT8020D11AQC (firmware revision 0114) implements (final-release) version 5.1 of G.723.1. Earlier versions of the CT8020 included pre-release versions of G.723.1 which are not directly compatible with the final v5.1 implementation. Transcoding between versions is possible using conversion software available from DSP Group. Below is a brief description of the G.723.1 revision history and its effect on the CT8020.

v3.0 September 1995 - used in initial CT8020A11AQC engineering samples

v4.0 January 1996 - approximately the same as v3.0 but with different bit packing structure for the compressed speech frames. This version is included in the CT8020A11BQC devices.

v4.1 April 1996 - fixed some instability problems in the G.723.1 algorithm encountered when pure sinewaves encoded.

v5.0 May 1996 - added silence compression VAD/CNG as Annex A of G.723.1. VAD = voice activity detection. CNG = comfort noise generation. This creates 4 possible speech frame sizes:
24 bytes 6.3 kbits/sec
20 bytes 5.3 kbits/sec
4 bytes CNG frame
1 byte silent frame

v5.1 Oct/Nov 1996, minor bug fix release affecting only the VAD feature. This version is implemented in the CT8020D11AQC

The main coder/decoder in the v5.1, v5.0 and v4.1 revisions are identical. When using the v5.1 coder with the VAD feature is disabled, the v5.1 and v4.1 encoders produce identical bit-streams. So inter-working between these versions of G.723.1 is straight forward.

It is possible to convert the compressed data between the various revisions so that, for example, chips to v3.0 can inter-work with v5.1. This requires software to run on the host. This is fairly simple code that re-packs bits and performs some table look-up operations on some bit-fields. DSP Group provides 'C' reference source code for use with the CT8020. This code may be freely incorporated into user software for use with CT8020 systems. DSP Group recommends that this code be incorporated into all software that works with the CT8020A11AQC and CT8020A11BQC devices to provide compatibility with the final G.723.1 v5.1 standard. Systems incorporating older versions of the G.723.1 standard should use the conversion software to promote to the final v5.1 G.723.1 version format.

Version 5.1 of G.723.1 has been approved by the ITU-T as the final version. There will be no further changes to this standard.

The changes introduced by the ITU in version 4.1 of G.723.1 necessitated equivalent changes to be made to the TrueSpeech 4.8 and 4.1 kbps speech coders. As a result of this conversion software must be included in order to enable inter-working between the (DSP Group proprietary) 4.8/4.1 rates in the A11AQC/A11BQC chips and the final CT8020D11AQC silicon.

G.723.1 Control Bits

Following are the control bit assignments as implemented in the various G.723.1 (pre-release) revisions:

v3.0 (**m.s**. 2 bits of first 16-bit word) CT8020A11AQC

bit 15	bit 14	
0	0	(reserved for silence, but not implemented)
0	1	6.3 rate
1	0	5.3 rate
1	1	(reserved)

v4.0 (**l.s.** 2 bits of first 16-bit word) CT8020A11BQC

bit 1	bit 0	
0	0	(reserved for silence, but not implemented)
0	1	5.3 rate
1	0	6.3 rate
1	1	(reserved)

v4.1 and v5.1 (**l.s.** 2 bits of first 16-bit word) - final formal release CT8020D11AQC

bit 1	bit 0	
0	0	6.3 rate
0	1	5.3 rate
1	0	4 byte silence frame (v5.1 only)
1	1	1 byte silence (not transmitted) frame (v5.1 only)

Ordering Information

CT8020D11AQC
128-pin PQFP Device with Commercial Temperature Range (0° - 70°C)

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DSP GROUP OFFICES

HEADQUARTERS
DSP Group, Inc.
3120 Scott Boulevard
Santa Clara, CA 95054
Telephone: (408) 986-4300
Facsimile: (408) 986-4490

JAPAN OFFICE
Nihon DSP Group, K.K.
Yasuda Kasai Building - 2nd Floor
2-3-1 Higashi-Gotanda
Shinagawa-ku, Tokyo 141-0022 JAPAN
Telephone: (81) 3-3449-7851
Facsimile: (81) 3-3449-8006

</div>

World Wide Web - http://www.dspg.com